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Subject Code:- AEC0502

Roll. No:

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NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech

SEM: V - CARRY OVER THEORY EXAMINATION - APRIL 2023

Subject: CMOS Digital Integrated Circuit

Time: 3 Hours

Max. Marks: 100

General Instructions:

IMP: Verify that you have received the question paper with the correct course, code, branch etc.

1. This Question paper comprises of **three Sections -A, B, & C.** It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.

2. Maximum marks for each question are indicated on right -hand side of each question.

3. Illustrate your answers with neat sketches wherever necessary.

4. Assume suitable data if necessary.

5. Preferably, write the answers in sequential order.

6. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION A

20

1. Attempt all parts:-

- 1-a. On what MOSFET working depend? (CO1) 1
- (a) MOS Transistor
 - (b) MOS Capacitor
 - (c) MOS Resistor
 - (d) MOS Voltage
- 1-b. What happens in the channel of enhancement MOSFET? If applied VGS below the threshold voltage. (CO1) 1
- (a) Conductivity Increased
 - (b) Conductivity decreased
 - (c) No channel detected
 - (d) Channel is fixed
- 1-c. The basic storage element in a digital system is _____. (CO2) 1
- (a) Flipflop
 - (b) Counter

- (c) Multiplexer
- (d) Encoder
- 1-d. The flash type A/D converters are called as _____. (CO2) 1
- (a) Parallel non-inverting A/D converter
- (b) Parallel counter A/D converter
- (c) Parallel inverting A/D converter
- (d) Parallel comparator A/D converter
- 1-e. The dynamic CMOS logic circuits operates in multiple phase, their noise immunity is _____. (CO3) 1
- (a) Frequency varying
- (b) Time varying
- (c) Always zero
- (d) Velocity varying
- 1-f. CMOS domino logic has _____. (CO3) 1
- (a) Smaller parasitic capacitance
- (b) Larger parasitic capacitance
- (c) Low operating speed
- (d) Very large parasitic capacitance
- 1-g. Vertical and horizontal directions in FPGA are separated by _____. (CO4) 1
- (a) A channel
- (b) A line
- (c) A flip-flop
- (d) A strobe
- 1-h. Design rules does not specify _____. (CO4) 1
- (a) linewidths
- (b) separations
- (c) extensions
- (d) colours
- 1-i. Which is not preferred for clock buffers? (CO5) 1
- (a) SVT
- (b) LVT
- (c) HVT
- (d) None

- 1-j. Explain the simulation mode which is used to check the timing performance of a design.(CO5) 1
- (a) Behavioural
 - (b) Switch-level
 - (c) Transistor-level
 - (d) Gate-level

2. Attempt all parts:-

- 2.a. Can a MOSFET conduct in both directions? Explain it. (CO1) 2
- 2.b. What are the applications of multiplexer circuit. (CO2) 2
- 2.c. How many transistors are needed to implement N-input function in Pseudo-NMOS logic? (CO3) 2
- 2.d. What are the characteristics of FPGA? (CO4) 2
- 2.e. What are the goals of floorplanning? (CO5) 2

SECTION B

30

3. Answer any five of the following:-

- 3-a. Define subthreshold conduction in MOSFET and derive the formula of subthreshold slope.(CO1) 6
- 3-b. Explain the channel pinched off condition in n-type MOSFET. (CO1) 6
- 3-c. Differentiate between combinational and sequential circuit design.(CO2) 6
- 3-d. Differentiate between a latch and a Flip-Flop.(CO2) 6
- 3.e. What makes dynamic CMOS circuits faster than static CMOS circuits? (CO3) 6
- 3.f. Design a stick diagram for CMOS based NAND gate. (CO4) 6
- 3.g. Write short note on Clock routing. (CO5) 6

SECTION C

50

4. Answer any one of the following:-

- 4-a. What are the critical voltages of a CMOS inverter? Derive the expressions for the critical voltages of a CMOS inverter. (CO1) 10
- 4-b. Calculate the critical voltages and noise margin for a CMOS inverter, if $V_{DD} = 3.3\text{ V}$, $V_{tn} = 0.3\text{ V}$, $V_{tp} = -0.3\text{ V}$, $\beta_n = 60\text{ }\mu\text{A/V}^2$, and $\beta_p = 20\text{ }\mu\text{A/V}^2$. Also calculate the power dissipation for a load of 0.1 pF and frequency of 100 MHz . (CO1) 10

5. Answer any one of the following:-

- 5-a. Implement the boolean expression $F(A, B, C) = \sum m(2, 3, 6, 7)$ using a multiplexer. (CO2) 10

5-b. Implement NAND gate JK flip-flop using CMOS and discuss its working. (CO2) 10

6. Answer any one of the following:-

6-a. How does the domino logic solves the problem in dynamic logic? (CO3) 10

6-b. Design and explain CMOS transmission gate full adder. (CO3) 10

7. Answer any one of the following:-

7-a. What is the purpose of design rule and stick diagram? What are the different approaches for describing the design rule? (CO4) 10

7-b. Draw the stick diagram and layout for CMOS Transmission Gate. (CO4) 10

8. Answer any one of the following:-

8-a. Explain in detail the floorplanning, placement and routing in ASIC design.(CO5) 10

8-b. Explain the steps needed to be taken care of while during floorplanning? (CO5) 10