Printed Page:- **Subject Code:- AEC0301**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech

SEM: III - CARRY OVER THEORY EXAMINATION - APRIL 2023

Subject: Digital System Design

Time: 3 Hours **Max. Marks: 100**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* **three Sections -A, B, & C.** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION A **20**

1. Attempt all parts:-

1-a. The logic expression AB + A' B' can be implemented by giving inputs A and B to a two-input (CO1) 1

(a) NOR gate

(b) XNOR gate

(c) XOR gate

(d) NAND gate

1-b. A bubble on the NOT gate input means (CO1) 1

(a) inversion OR

(b) Double inversion

(c) inversion AND

(d) Complement

1-c. The binary subtraction 0 – 1 = (CO2) 1

(a) difference = 0, borrow = 0

(b) difference = 1, borrow = 0

COP 2022-23 July_Dec

(c) difference = 1, borrow =1

(d) difference = 0, borrow = 1

1-d. Which combinational circuit is selecting a single input from multiple inputs & directing the binary information to output line? (CO2) 1

(a) Multiplexer

(b) Data distributor

(c) Both data selector and data distributor

(d) DeMultiplexer

1-e. Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature? (CO3) 1

(a) Low input voltages

(b) Synchronous operation

(c) Gate impedance

(d) Cross coupling

1-f. When is a flip-flop said to be transparent? (CO3) 1

(a) When the Q output is opposite the input

(b) When the Q output follows the input

(c) When you can see through the IC packaging

(d) When the Q output is complementary of the input

1-g. Recommended Fanout for TTL gate. (CO4) 1

(a) 10

(b) 40

(c) 60

(d) 50

1-h. Which is not the state of TTL tristate output? (CO4) 1

(a) LOW

(b) High

(c) High Impedance

(d) Low Impedance

1-i. PLA Consist of ..... (CO5) 1

(a) Programable AND and Programable OR Arrays

(b) Programable AND and Fixed OR Arrays

(c) Fixed AND and Programable OR Arrays

COP 2022-23 July_Dec

(d) Fixed AND and Fixed OR Arrays

1-j. In which type of ROM, data can be erased by ultraviolet light and then reprogrammed by the user or manufacturer? (CO5) 1

(a) PROM

(b) EPROM

(c) EEPROM

(d) Both a and b

2. Attempt all parts:-

2.a. Perform the subtraction of 8 - 5 using 1's complement. (CO1) 2

2.b. Design one bit magnitude comparator. (CO2) 2

2.c. Write the characteristic equation and excitation table of J K flip-flop. (CO3) 2

2.d. Explain the operation of 2-input TTL NAND gate. (CO4) 2

2.e. Compare RAM with ROM. (CO5) 2

SECTION B **30**

3. Answer any <u>five</u> of the following:-

3-a. If A=1011 and B= 1110 using 2's complement, Find A-B= ? (CO1) 6

3-b. Find the Boolean expression in SOP form of 3 inputs NAND and NOR gate using K—map? (CO2) 6

3-c. Implement the Boolean function f (A,B,C,D) = ∑(2,4,6,9,10,11,13) with 8:1 multiplexers. (CO2) 6

3-d. Design a 4 bit binary to gray code converter. (CO2) 6

3.e. Convert J K flip flop into D flip flop. (CO3) 6

3.f. Compare TTL , ECL and CMOS logic families. (CO4) 6

3.g. Draw block diagram of PLA and explain function of each block. (CO5) 6

SECTION C **50**

4. Answer any <u>one</u> of the following:-

4-a. What is Hamming Code? Generate Hamming code for data 1011 assuming even parity. (CO1) 10

4-b. Realize the OR and XOR logic operation using NAND gates. (CO1) 10

5. Answer any <u>one</u> of the following:-

5-a. Design a full adder using two half adder. (CO2) 10

5-b. Design one digit BCD Adder using IC 7483. (CO2) 10

COP 2022-23 July _ Dec

6. Answer any <u>one</u> of the following:-

6-a.	Design a Mod-10 synchronous counter. (CO3)	10
6-b.	Explain Johnson counter in detail. (CO3)	10

7. Answer any <u>one</u> of the following:-

7-a.	Draw the basic gate of ECL and explain its operation. (CO4)	10
7-b.	Draw the basic gate of COMS and explain its operation. (CO4)	10

8. Answer any <u>one</u> of the following:-

8-a.	Implement Full adder circuit using PLA. (CO5)	10
8-b.	Design Logic circuit using PLD which can perform the following functions: Z1 = WX'Y' + WXY' + WXY, Z2 = W'XY + WX'Y + WXY, Z3 = W'XY + WX'Y' + W'XY' (CO5)	10

COP 2022-23 July_Dec