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Printed	Page:- Subject Code:- ACSBS0303
	Roll. No:
	NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA
	(An Autonomous Institute Affiliated to AKTU, Lucknow)
	B.Tech
	SEM: III - CARRY OVER THEORY EXAMINATION - APRIL 2023
	Subject: Computer Organization & Architecture
Time:	3 Hours Max. Marks: 100
	Instructions:
	ify that you have received the question paper with the correct course, code, branch etc.
	Duestion paper comprises of three Sections -A, B, & C. It consists of Multiple Choice
	s (MCQ's) & Subjective type questions.
	num marks for each question are indicated on right -hand side of each question.
	ate your answers with neat sketches wherever necessary.
	e suitable data if necessary.
•	ably, write the answers in sequential order. neet should be left blank. Any written material after a blank sheet will not be
	d/checked.
evaluate	
	SECTION A 20
1. Atten	npt all parts:-
1-a.	Brain of computer is (CO1)
	(a) Control unit
	(b) Arithmetic and Logic unit
	(c) Central Processing Unit
	(d) Memory
1-b.	bus arbitration approach uses the involvement of processor. (CO1)
	(a) Centralized
	(b) Distributed
	(c) Randomized
	(d) All of the mentioned
1-c.	One way to make an adder to perform subtraction is by (CO2)
	(a) Inverting the output
	(b) Inverting the carry-in
	(c) Inverting the B inputs

	(d) Grounding the B inputs	
1-d.	For a 4-bit parallel adder, if the carry-in is connected to a logical HIGH, the result is (CO2)	e 1
	(a) The same as if the carry-in is tied LOW since the least significant carr ignored	y-in is
	(b) That carry-out will always be HIGH	
	(c) A one will be added to the final result	
	(d) The carry-out is ignored	
1-e.	Which of the following is fastest memory? (CO3)	1
	(a) Secondary memory	
	(b) Auxiliary memory	_(
	(c) Cache memory	
	(d) Virtual memory	
1-f.	The instruction JUMP belongs to (CO3)	1
	(a) Data transfer instruction	
	(b) Branch instruction	
	(c) Logical instruction	
	(d) Arithmetic instruction	
1-g.	Which interrupt is non-maskable? (CO4)	1
	(a) RST 7.5	
	(b) RST 5.5	
	(c) TRAP	
	(d) INTR	
1-h.	How many types of modes are present in I/O Data Transfer? (CO4)	1
	(a) 3	
	(b) 2	
	(c) 5	
	(d) 4	
1-i.	have been developed specifically for pipelined systems. (CO5)	1
	(a) Utility software	
	(b) Speed up utilities	
	(c) Optimizing compilers	
	(d) None of the mentioned	

1-j.	Which of the following page replacement algorithms suffers from Belady's Anomaly? (CO5)	1
	(a) Optimal replacement	
	(b) LRU	
	(c) FIFO	
	(d) Both optimal replacement and FIFO	
2. Atten	npt all parts:-	
2.a.	Define system bus. (CO1)	2
2.b.	What is an overflow? (CO2)	2
2.c.	Explain the functionality of RAM chip. (CO3)	2
2.d.	Explain software interrupts. (CO4)	2
2.e.	What are the different factors that can affect the performance of pipeline system? (CO5)	2
	SECTION B	30
3. Answ	er any <u>five</u> of the following:-	
3-a.	Explain input-output subsystems and control unit in computer system. (CO1)	6
3-b.	What are the various addressing modes available in computer system? Explain with example. (CO1)	6
3-c.	Explain the Signed magnitude multiplication algorithm with the help of flow chart. (CO2)	6
3-d.	Perform multiplication of (-9) with (-13) using booth's algorithm. (CO2)	6
3.e.	Explain the concept of hierarchical memory organization with the help of diagram. (CO3)	6
3.f.	What is DMA? Explain DMA transfer in a computer system with the help of diagram. (CO4)	6
3.g.	Describe the basic concept of Pipelining. Write any two Disadvantages of Pipelining. (CO5)	6
	SECTION C	50
4. Answ	er any <u>one</u> of the following:-	
4-a.	Explain various functional blocks of a computer in detail with block diagram. (CO1)	10
4-b.	Explain Applications of Multiplexer in details. (CO1)	10
5. Answ	er any one of the following:-	

5-a.	What is IEEE 754 Floating point representation? Explain single-precision and double-precision Floating point representation with example. (CO2)	10
5-b.	Draw the architecture of 8086 microprocessor and explain it also. (CO2)	10
6. Answ	er any <u>one</u> of the following:-	
6-a.	What is cache memory? Explain various mapping techniques available in cache memory. (CO3)	10
6-b.	What are the three types of instruction format? Explain in details with example. (CO3)	10
7. Answ	er any <u>one</u> of the following:-	
7-a.	What are the various I/O transfers? Explain I/O device interface with block diagram. (CO4)	10
7-b.	Why Handshaking is required in asynchronous data transfer? Explain. (CO4)	10
8. Answ	er any <u>one</u> of the following:-	
8-a.	What is Parallel processing? Also differentiate between pipelining and parallel processing. (CO5)	10
8-b.	What is Concurrent access to memory and cache coherency? Explain in detail. (CO5)	10