Printed page: 3 **Subject Code**: AEC0502

Roll No: | | | | | | | | | | | | | |

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B. Tech

(SEM: V, THEORY EXAMINATION (2022-2023)

Subject: CMOS Digital Integrated Circuit

Time: 3 Hours Max. Marks:100

General Instructions:

IMP: Verify that you have received question paper with correct course, code, branch etc.

1. *This Question paper comprises of three Sections -A, B, & C. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*
2. *Maximum marks for each question are indicated on right hand side of each question.*
3. *Illustrate your answers with neat sketches wherever necessary.*
4. *Assume suitable data if necessary.*
5. *Preferably, write the answers in sequential order.*
6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION – A 20

1. Attempt all parts:-

1-a. Time for which data should remain valid after the clock edge is called as (CO1) 1
A. Set up time
B. Hold time
C. Propagation Delay
D. Critical Delay

1-b. In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance? (CO1) 1
A. Static dissipation
B. Dynamic dissipation
C. Both a and b
D. None of the above

1-c. The practical use of binary-weighted digital-to-analog converters is limited to 1
A. R/2R ladder D/A converters (CO2)
B. 4-bit D/A converters
C. 8-bit D/A converters
D. Op-amp comparators

1-d. The basic storage element in a digital system is _____ (CO2) 1
A. Flip Flop
B. Counter
C. Multiplexer
D. Encoder

1-e. The designing of address decoders in memory chips can be done in (CO3) 1
A. TTL Logic
B. PTL Logic
C. Domino CMOS Logic
D. CMOS Logic

1-f.	Power dissipation in absence of any switching activity is defined as (CO3) A. Dynamic power consumption B. Leakage power consumption C. Static power consumption D. Direct path power Consumption	1
1-g.	n and p transistors are separated by using ____ (CO4) A. Differential line B. Separation Line C. Demarcation Line D. Back Line	1
1-h.	What is the design flow of VLSI system? (CO4) A. market requirement, architecture design, logic design, HDL coding B. architecture design, market requirement, logic design, HDL coding C. logic design, architecture design, HDL coding, market requirement D. HDL coding, logic design, architecture design, market requirement	1
1-i.	_____ is a programmable ASIC. (CO5) A. Cell Based ASIC B. Full Custom ASIC C. Field programmable Gate array based ASIC D. Structured Gate Array based ASIC	1
1-j.	In floor-planning, placement and routing are _____ tools. (CO5) A. Front End B. Back end C. Both a and b D. None of the above	1
2. Attempt all parts:-		
2.a.	What is the relation between input and output voltage of CMOS inverter at threshold voltage? (CO1)	2
2.b.	What is the major disadvantage of dual-slope type ADC? (CO2)	2
2.c.	Write two major disadvantages of Pseudo-NMOS logic. (CO3)	2
2.d.	What is the difference between stick diagram and layout diagram? (CO4)	2
2.e.	What is Layout Vs Schematic (LVS)? (CO5)	2
	SECTION – B	**30**
3. Answer any five of the following-		
3-a.	Explain and derive MOS I/V characteristics and plot its drain-current versus drain- source voltage in the triode and saturation region. (CO1)	6
3-b.	Explain the working of a CMOS inverter. Also derive its transfer characteristics. (CO1)	6
3-c.	Explain in brief the successive Approximation Register (SAR). (CO2)	6
3-d.	Explain working of CMOS Half adder with the help of a neat diagram. (CO2)	6
3-e.	List the advantage of Domino logic and explain its working with an example. (CO3)	6
3-f.	Explain the concept of regularity, modularity & locality. (CO4)	6
3-g.	What is the different verification methodologies used in VLSI design flow, explain it with suitable flow diagram? (CO5)	6
	SECTION – C	**50**
4. Answer any one of the following-		
4-a.	Calculate the drain current of an NMOS transistor with following parameters: βn = 60 μA/V2, VGS = 1.0 V, VDS = 1.5 V, Vt0 = 0.6 V. (CO1)	10
4-b.	Explain the channel length modulation effect and derive an expression for saturated drain current considering channel length modulation. (CO1)	10
5. Answer any one of the following-		
5-a.	An 8-bit DAC has an output of 3.92 mA for an input of 01100010. What are the DAC's resolution and full-scale output? (CO2)	10

5-b.	Draw a block diagram of a Flash type ADC and discuss its advantages and limitations. (CO2)	10
6.	Answer any one of the following-	
6-a.	Explain the structure of the CMOS transmission gate. Plot the equivalent resistance of CMOS Transmission gate as a function of the output voltage and describe its three regions of operation with relevant equations. (CO3)	10
6-b.	Explain the cascading problem and charge sharing in dynamic CMOS logic. (CO3)	10
7.	Answer any one of the following-	
7-a.	What do you mean by design rules? Discuss different design rules with examples. (CO4)	10
7-b.	Explain the procedure for measurement of delay in floor planning. (CO4)	10
8.	Answer any one of the following-	
8-a.	Explain various stages of ASIC design flow. Describe the various parameters considered for ASIC variable cost. (CO5)	10
8-b.	What is the role of testing in VLSI circuits? Illustrate the difference between analog and digital testing. (CO5)	10