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NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech

(SEM: III THEORY EXAMINATION (2022-2023))

Subject : Digital System Design

Time: 3Hours

Max. Marks:100

General Instructions:

IMP: Verify that you have received question paper with correct course, code, branch etc.

1. *This Question paper comprises of three Sections -A, B, & C. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*
2. *Maximum marks for each question are indicated on right hand side of each question.*
3. *Illustrate your answers with neat sketches wherever necessary.*
4. *Assume suitable data if necessary.*
5. *Preferably, write the answers in sequential order.*
6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION – A

20

1. Attempt all parts:-

- | | | |
|------|---|---|
| 1-a. | If , $(45)_{10} = (55)_b$, the possible base b is ---. (CO1) | 1 |
| | (a). 3 | |
| | (b). 4 | |
| | (c). 5 | |
| | (d). 8 | |
| 1-b. | A message bit is 010101. We are using even parity generator, so that the parity bit added to the message bit is (CO1) | 1 |
| | (a). 0 | |
| | (b). 1 | |
| | (c). 0 & 1 | |
| | (d). None of these. | |
| 1-c. | Number of half and full adders are required to construct a 64-bit binary adder would be (CO2) | 1 |
| | (a). One half- adder and 63 full-adders | |
| | (b). 64 full-adders | |
| | (c). 64 half- adder | |
| | (d). 63 half- adders and one full-adder. | |
| 1-d. | A code used for labelling the cells of a K-map is (CO2) | 1 |
| | (a). 8-4-2-1 binary | |
| | (b). Hexadecimal | |
| | (c). Gray | |

- (d). Octal.
- 1-e. A shift counter comprising of a cascaded arrangement of five flip-flops with inverse feedback from output of MSB flip-flop to input of LSB flip-flop is a (CO3) 1
- (a). Divide-by-32-counter
(b). Divide-by-10-counter
(c). Divide-by-5-counter
(d). Five bit shift register
- 1-f. In mealy circuit the output depends on ----- (CO3) 1
- (a). Both states and inputs
(b). Only on inputs
(c). Only on states
(d). None of the above.
- 1-g. Which logic family has the lowest noise immunity? (CO4) 1
- (a). TTL
(b). ECL
(c). CMOS
(d). NMOS
- 1-h. Of the various commonly used logic families, the one with highest speed and one with least power dissipation, respectively, are (CO4) 1
- (a). TTL and CMOS
(b). CMOS and TTL
(c). CMOS and ECL
(d). ECL and CMOS
- 1-i. In PLA, AND gate array and OR gate array are----- respectively. (CO5) 1
- (a). Fixed and Programmable
(b). Programmable and Programmable
(c). Fixed and Fixed.
(d). Programmable and Fixed
- 1-j. Which is a non-volatile memory?. (CO5) 1
- (a). SRAM
(b). DRAM
(c). ROM
(d). None of the above
2. Attempt all parts:-
- 2.a. Perform the BCD addition $568 + 679 = ?$. (CO1) 2
- 2.b. Write the output expressions of a 4bit magnitude comparator. (CO2) 2
- 2.c. What is the difference between truth table and excitation table? (CO3) 2
- 2.d. Define the following terms with suitable example (CO4) 2
- (i)-Noise immunity, (ii)- Fanout (iii)- transition time and (iv)- propagation delay.
- 2.e. Compare EPROM with EEPROM. (CO5) 2

SECTION – B

3. Answer any five of the following- 30
- 3-a. Why are NAND and NOR gates known as universal gates? Prove your answer with proper reasoning. (CO1) 6

3-b.	Perform the subtraction $A-B = ?$ and $B-A = ?$ For $A=1100$ and $B=1001$ using 2's complement. (CO1)	6
3-c.	Design and draw a 2-bit magnitude comparator circuit. (CO2)	6
3-d.	Simplify the following Boolean expression using K-map $F(A, B, C, D) = \sum m(0, 1, 3, 6, 7, 8, 9, 12, 14, 15)$ (CO2)	6
3-e.	Show that the characteristic equation for the complement output of a J-K flip flop is $Q'(t+1) = J'Q' + KQ$. (CO3)	6
3-f.	Draw the basic Gate of ECL logic family and explain its operation with advantages and disadvantages. (CO4)	6
3-g.	Given the function $f(x_1, x_2, x_3) = \sum(2, 3, 4, 6, 7)$ Show how it can be realized using two 2-input LUTs. Give the truth table implemented in each LUT. (CO5)	6
SECTION – C		50
4.	Answer any <u>one</u> of the following-	
4-a.	Determine the single-error-correcting code (hamming code) for the BCD number 1001 (information bits), using even parity. (CO1)	10
4-b.	Implement Boolean expression using only NOR gates (CO1) $\overline{((A+B)C)}D$	10
5.	Answer any <u>one</u> of the following-	
5-a.	Simplify the following Boolean expression using tabulation method or K Map. $F = \sum m(0, 1, 9, 15, 24, 29, 30) + d(8, 11, 31)$ (CO2)	10
5-b.	Implement the following function $F(A, B, C, D) = \sum m(0, 1, 3, 4, 7, 8, 9, 11, 14, 15)$ Using 8:1 MUX (CO2)	10
6.	Answer any <u>one</u> of the following-	
6-a.	Design MOD-5 synchronous counter using J-K flip flop and implement it. (CO3)	10
6-b.	Explain the working of recirculating shift registers, why should shift register stages be edge triggered? Illustrate its propagation delay. (CO3)	10
7.	Answer any <u>one</u> of the following-	
7-a.	Draw the internal structure of a TTL tristate gate and explain its operation. Explain with proper reasons, why active pull up and pull down are preferred over passive and also compare TTL gates with MOS gate. (CO4)	10
7-b.	Draw the basic gates of CMOS logic family and explain the operations with truth tables. (CO4)	10
8.	Answer any <u>one</u> of the following-	
8-a.	Design a combinational logic circuit having 4 inputs and two outputs F_1 and F_2 . The output F_1 gives high output when the input combinational is greater than or equal to 1001, otherwise low output. The output F_2 gives high output when the input combinational is less than 1001 otherwise the output F_2 is LOW. (CO5)	10
8-b.	Draw the Block diagram of PLA and also, design a full adder circuit using PLA. (CO5)	10