Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech

SEM: III - THEORY EXAMINATION (2022 - 2023)

Subject: Computer Organization & Architecture

Time: 3 Hours   Max. Marks: 100

General Instructions:

IMP: Verify that you have received the question paper with the correct course, code, branch etc.

1. This Question paper comprises of three Sections -A, B, & C. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.

2. Maximum marks for each question are indicated on right -hand side of each question.

3. Illustrate your answers with neat sketches wherever necessary.

4. Assume suitable data if necessary.

5. Preferably, write the answers in sequential order.

6. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

<div align="center">SECTION A   20</div>

1. Attempt all parts:-

1-a.   The operation of insertion in stack is called _____.   (CO1)   1

               (a) PUSH

               (b) POP

               (c) Addressing

               (d) None

1-b.   The addressing mode in which the operands are specified implicitly in the instruction.   1
(CO1)

               (a) Indirect addressing mode

               (b) Index addressing mode

               (c) Relative addressing mode

               (d) Implied addressing mode

1-c.   When we perform subtraction on -7 and 1 the answer in 2's complement form   1
is_____.   (CO2)

               (a) 1010

(b) 1110

(c) 110

(d) 1000

1-d.   IEEE 754 representation for _____.   (CO2)   1

(a) Floating Point No.

(b) Integer no.

(c) Binary no.

(d) Octal no.

1-e.   What does the hardwired control generator consists?   (CO3)   1

(a) Decoder/encoder

(b) Condition codes

(c) Control step counter

(d) All of the mentioned

1-f.   How many address bits are required to represent a 32 K memory?   (CO3)   1

(a) 10 bits

(b) 12 bits

(c) 14 bits

(d) 15 bits

1-g.   Which of the following is true?   (CO4)   1

(a) To overcome the slow operating speeds of the secondary memory we make use of faster flash drives.

(b) If we use the flash drives instead of the hard disks, then the secondary storage can go above primary memory in the hierarchy.

(c) In the memory hierarchy, as the speed of operation increases the memory size also increases

(d) None

1-h.   Time for replacing the block from memory, is referred as_____.   (CO4)   1

(a) miss penalty

(b) Penalty

(c) Hit

(d) Miss

1-i.   The technique whereby the DMA controller steals the access cycles of the processor to   1

operate is called _____.   (CO5)

        (a) Memory stealing

        (b) Memory Con

        (c) Cycle stealing

        (d) Fast conning

1-j.   A hand-shake based protocol for data transfer is an example of _____ type of data transfer.   (CO5)   1

        (a) Parallel

        (b) Synchronous

        (c) Asynchronous

        (d) Serial

2. Attempt all parts:-

2.a.	What is three-state buffer. Draw the symbol. (CO1)	2
2.b.	Explain the hardware diagram of signed magnitude multiplication algorithm. (CO2)	2
2.c.	Give two examples of microoperations performed by CPU. (CO3)	2
2.d.	What do you mean by address space and memory space in virtual memory? (CO4)	2
2.e.	Write the difference between serial and parallel communication. (CO5)	2

<div align="center">SECTION B   30</div>

3. Answer any <u>five</u> of the following:-

3-a.	What is register and how register transfer process is done? Explain with the help of Block diagram and timing diagram. (CO1)	6
3-b.	Draw the diagram of bus system that uses three state buffers and 2:4 decoder instead of multiplexers and Explain how it works. (CO1)	6
3-c.	Differentiate between single precision and double precision representation of floating point number in tabular form. (CO2)	6
3-d.	Solve -15 X +13 using booth algorithm. Assume 5 bit registers that hold signed numbers. (CO2)	6
3.e.	Evaluate the arithmetic expression X = (A + B) * (C + D) using two address and three address instructions. (CO3)	6
3.f.	Define set associative mapping in cache memory. (CO4)	6
3.g.	Differentiate between synchronous and asynchronous data transfer. (CO5)	6

<div align="center">SECTION C   50</div>

4. Answer any <u>one</u> of the following:-

4-a.   Explain seven registers CPU organization with the help of block diagram and control   10
            word.   (CO1)

4-b.   What is Bus Arbitration and its types? Why it is required? .   (CO1)   10

5. Answer any <u>one</u> of the following:-

5-a.   Sketch the array multiplier of 4 bit binary numbers, multiplicand is (b3 b2 b1 b0) &   10
            multiplier is (a2 a1 a0) with AND gates and full adders.   (CO2)

5-b.   Explain Division algorithm step-wise with the help of suitable example.   (CO2)   10

6. Answer any <u>one</u> of the following:-

6-a.   What is hardwired control logic? Explain using neat sketch.   (CO3)   10

6-b.   Design and explain the concept of Pipelining with the help of suitable example.   (CO3)   10

7. Answer any <u>one</u> of the following:-

7-a.   How the mapping is done between cache and main memory? Explain at least two methods of   10
            mapping.   (CO4)

7-b.   Make a neat sketch of 1024 X 8 memory system connection to the CPU using four RAM   10
            chips and one ROM chip and explain about connections.   (CO4)

8. Answer any <u>one</u> of the following:-

8-a.   What is DMA? Describe how DMA controller is used to transfer data from peripherals to   10
            memory.   (CO5)

8-b.   Explain the different modes of data transfer in detail.   (CO5)   10