Printed Page:- Subject Code:- ACSBS0303

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B,Tech.

SEM: III - THEORY EXAMINATION (2022 - 2023)

Subject: Computer Organization & Architecture

Time: 3 Hours Max. Marks: 100

General Instructions:

IMP: Verify that you have received the question paper with the correct course, code, branch etc.

1. This Question paper comprises of three Sections -A, B, & C. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.

2. Maximum marks for each question are indicated on right -hand side of each question.

3. Illustrate your answers with neat sketches wherever necessary.

4. Assume suitable data if necessary.

5. Preferably, write the answers in sequential order.

6. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION A 20

1. Attempt all parts:-

1-a. A special request originated from some device to the CPU to acquire some of its time is called _____ . (CO1) 1

(a) Disturbance

(b) Attenuation

(c) Interrupt

(d) Noise

1-b. Components that provide internal storage to the CPU are _____. (CO1) 1

(a) Registers

(b) Program Counters

(c) Controllers

(d) Internal chips

1-c. _____ is responsible for arithmetic operation. (CO2) 1

(a) Control unit

(b) ALU

(c) Memory unit

(d) I/O unit

1-d. Which flag indicates the number of 1 bit that results from an operation? (CO2) 1

(a) Zero

(b) Parity

(c) Auxiliary

(d) Carry

1-e. Property of locality of reference may fail, if a program has_____. (CO3) 1

(a) many conditional jumps

(b) many unconditional jumps

(c) many operand

(d) many operators

1-f. The next level of memory hierarchy after the L2 cache is _____. (CO3) 1

(a) Secondary storage

(b) Main memory

(c) Register

(d) TLB

1-g. A _____ command is issued to activate the peripheral and to inform it what to do. (CO4) 1

(a) Control

(b) Status

(c) Data output

(d) Data Input

1-h. After the completion of the DMA transfer, the processor is notified by _____. (CO4) 1

(a) Acknowledge signal

(b) Interrupt signal

(c) WMFC signal

(d) None of the mentioned

1-i. To increase the speed of memory access in pipelining, we make use of _____. (CO5) 1

(a) Special memory locations

(b) Special purpose registers

(c) Cache

(d) Buffers

1-j. The computer architecture aimed at reducing the time of execution of instructions is _____. (CO5) 1

(a) CISC

(b) RISC

(c) ISA

(d) ANNA

2. Attempt all parts:-

2.a. Why Bus arbitration is required? (CO1) 2

2.b. Explain the Advantages and Disadvantages of CLA Adder. (CO2) 2

2.c. Describe the concept of memory hierarchy. (CO3) 2

2.d. Describe Programmed I/O mode of transfer. (CO4) 2

2.e. Why do we need stalling in pipelining process? (CO5) 2

SECTION B 30

3. Answer any five of the following:-

3-a. Explain the different type of Bus structures for interconnecting functional units along with diagram. (CO1) 6

3-b. Explain the following addressing modes with examples- 6

i. Register Indirect addressing

ii) Relative Addressing

iii. Indirect Addressing

iii) Direct Addressing. (CO1)

3-c. Draw the Booth multiplication algorithm flow diagram and explain it in detail. (CO2) 6

3-d. Explain single precision and double precision IEEE 754 representation for -2.35. (CO2) 6

3.e. What is associative memory mapping in cache memory? Explain with the help of diagram. (CO3) 6

3.f. What is Interrupt? Explain the different types of Interrupts. (CO4) 6

3.g. What is Arithmetic Pipeline? Explain with example. (CO5) 6

SECTION C 50

4. Answer any one of the following:-

4-a. Explain bus organization for seven CPU registers with the help of block diagram and control 10

word. (CO1)

4-b. What is Stack organization? Explain Memory Stack organization. (CO1) 10

5. Answer any one of the following:-

5-a. Solve +15 X +13 using Signed magnitude algorithm. Assume 5-bit registers that hold signed numbers. (CO2) 10

5-b. Draw the architecture of 8086 microprocessor. Explain segments in 8086 microprocessor also. (CO2) 10

6. Answer any one of the following:-

6-a. Why micro-programmed control is better than hardwired control unit? Identify some situations when hardwired is preferred? (CO3) 10

6-b. What is cache memory? Explain its replacement algorithms also. (CO3) 10

7. Answer any one of the following:-

7-a. Differentiate between memory mapped I/O and I/O mapped I/O. Explain with block diagram. (CO4) 10

7-b. What is ISR? Explain the action carried out by the processor after occurrence of an interrupt. (CO4) 10

8. Answer any one of the following:-

8-a. What is difference between pipeline and parallel processing? Explain with the help of block diagram. (CO5) 10

8-b. Explain different types of pipeline hazards. Explain how to resolve them. (CO5) 10