Printed Page:- Subject Code:- ACSAI0302

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech

SEM: III - THEORY EXAMINATION (2022 - 2023)

Subject: Logic Design and Computer Architecture

Time: 3 Hours Max. Marks: 100

General Instructions:

IMP: Verify that you have received the question paper with the correct course, code, branch etc.

1. This Question paper comprises of three Sections -A, B, & C. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.

2. Maximum marks for each question are indicated on right -hand side of each question.

3. Illustrate your answers with neat sketches wherever necessary.

4. Assume suitable data if necessary.

5. Preferably, write the answers in sequential order.

6. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION A 20

1. Attempt all parts:-

1-a. Register is a type of _____ circuit. (CO1) 1

(a) Addder

(b) Sequential

(c) Combinational

(d) None

1-b. Which of the following is a combinational circuit which has 1 output? (CO1) 1

(a) Demultiplexer

(b) Multiplexer

(c) Counter

(d) Decoder

1-c. IEEE 754 representation for _____. (CO2) 1

(a) Floating Point No.

(b) Integer no.

(c) Binary no.

(d) Octal no.

1-d. Carry lookahead adder uses the concepts of _____. (CO2) 1

(a) Inverting the inputs

(b) Complementing the outputs

(c) Generating and propagating carries

(d) None of the mentioned

1-e. Highly encoded schemes that use compact codes to specify a small number of functions in each micro instruction is_____. (CO3) 1

(a) Horizontal organisation

(b) Vertical organisation

(c) Diagonal organisation

(d) None of the mentioned

1-f. What is SIMD in parallel processing? (CO3) 1

(a) Single instruction stream, mega data stream

(b) Sequence instruction stream, multiple data stream

(c) Separate instruction stream, multiple data stream

(d) Single instruction stream, multiple data stream

1-g. What is the formula for Hit Ratio? (CO4) 1

(a) Hit/(Hit + Miss)

(b) Miss/(Hit + Miss)

(c) (Hit + Miss)/Miss

(d) (Hit + Miss)/Hit

1-h. The transformation of data from main memory to cache memory is referred to as a _____ process. (CO4) 1

(a) hit

(b) miss

(c) mapping

(d) None of the above

1-i. The _____ is defined as the rate at which serial information is transmitted and is equivalent to the data transfer in bits per second. (CO5) 1

(a) Stop bit

(b) Start bit

(c) Read bit

(d) Baud rate

1-j. A hand-shake based protocol for data transfer is an example of _____ type of data transfer. (CO5) 1

(a) Parallel

(b) Synchronous

(c) Asynchronous

(d) Serial

2. Attempt all parts:-

2.a. A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. a) How many multiplexers are there in the bus? b) What size of multiplexers are needed? (CO1) 2

2.b. What is the value of 11010010 after arithmetic shift left and right? (CO2) 2

2.c. Explain micro-instruction format with diagram. (CO3) 2

2.d. Define the term page frame. (CO4) 2

2.e. Write down the difference between Isolated I/O and Memory mapped I/O. Also discuss the advantages and disadvantages of both. (CO5) 2

SECTION B 30

3. Answer any five of the following:-

3-a. Draw the diagram of bus system that uses three state buffers and 2:4 decoder instead of multiplexers and Explain how it works. (CO1) 6

3-b. What is register and how register transfer process is done? Explain with the help of Block diagram and timing diagram. (CO1) 6

3-c. Sketch the flow diagram of division algorithm with suitable example. (CO2) 6

3-d. Explain the concept of Multiplication with various algorithm. (CO2) 6

3.e. Evaluate the arithmetic expression X = (A + B) * (C + D) using two address instructions. (CO3) 6

3.f. Give formula to calculate average memory access time. (CO4) 6

3.g. List the instructions to be written in initial sequence of each interrupt service routines to control the interrupt hardware. (CO5) 6

SECTION C 50

4. Answer any one of the following:-

4-a.	Describe various addressing techniques with the help of examples. (CO1)	10
4-b.	What is Bus Arbitration? Why it is required? Explain its types. (CO1)	10

5. Answer any one of the following:-

5-a.	Explain the IEEE 754 floating point representation with examples. (CO2)	10
5-b.	Explain the working of 4 bit Carry Look Ahead Adder with help of example. (CO2)	10

6. Answer any one of the following:-

6-a.	What is micro program sequencer? Explain using neat sketch. (CO3)	10
6-b.	Explain flowchart for instruction cycle with neat diagram. (CO3)	10

7. Answer any one of the following:-

7-a.	Discuss the different mapping techniques used in cache memories and their relative merits and demerits. (CO4)	10
7-b.	Explain chip interconnections when 1024 X 8 memory is constructed using 128 X 8 RAM chips and 512 X 8 ROM chips. (CO4)	10

8. Answer any one of the following:-

8-a.	Explain various modes of data transfer between processor and peripheral devices. (CO5)	10
8-b.	Explain how DMA transfer is accomplished with the help of diagram. (CO5)	10