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NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA (An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech

Roll. No:

Subject Code:- AMTVL0114

SEM: I - THEORY EXAMINATION (2022 - 2023) Subject: Microchip Fabrication Technology

Time: 3 Hours

General Instructions:

IMP: Verify that you have received the question paper with the correct course, code, branch etc.

1. This Question paper comprises of **three Sections -A**, **B**, **& C**. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. Assume suitable data if necessary.

5. *Preferably, write the answers in sequential order.*

6. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION A

1. Attempt all parts:-

- 1-a. Which of these cannot be fabricated on an IC? (CO1)
 - (a) Transistors
 - (b) Diodes
 - (c) Registers
 - (d) Large inductors and transformers

1-b. SiO2 acts as : (CO2)

(a) Conductor

(b) Semiconductor

- (c) Insulator
- (d) None of these
- 1-c. Photolitography (CO3)

(a) Patterning process that transfers the designed pattern from the mask or reticle to the wafer surface

(b) Patterning process that transfers the designed pattern from the mask or

Max. Marks: 70

1

1

1

15

reticle to the substrate

(c) Patterning process that transfers the designed pattern from the mask or reticle to the photoresist on the wafer surface

(d) Patterning process that transfers the designed pattern from the mask or reticle to the photoresist on the back side substrate

1

- 1-d. Impurity diffusion is used in semiconductor to control the conductivity. (CO4) 1
 - (a) TRUE
 - (b) FALSE
- 1-e. The ohmic contacts are deposited by (CO5)
 - (a) decomposition
 - (b) evaporation
 - (c) deposition
 - (d) mixing

2. Attempt all parts:-

2.a.	Give two reasons silicon is the most common semiconducting material. (CO1)	2	
2.b.	Sketch a cubic unit cell and identify the <100> plane. (CO2)	2	
2.c.	List four differences between optical lithography and electron beam lithography? (CO3)	2	
2.d.	What is Ion-Implantation Technique? Discuss in brief. (CO4)	2	
2.e.	List the four functions of a semiconductor package. (CO5)	2	
	SECTION B	20	
3. Answe	er any <u>five</u> of the following:-		
З-а.	Explain various point defects. (CO1)	4	
3-b.	Explain process of obtaining MGS from sand. (CO1)	4	
3-c.	Draw a sketch of a horizontal tube furnace and identify all the sections. (CO2)	4	
3-d.	Explain principle uses of Si dioxide (SiO2) layer in Si wafer devices. (CO2)	4	
3.e.	Discuss positive photo resist with suitable diagram. (CO3)	4	
3.f.	Describe in detail Plasma enhanced CVD systems. (CO4)	4	
3.g.	What are the advantages of a sputter process compared to an evaporator process? (CO5)	4	
	SECTION C	35	
A Answer any one of the following:			

4. Answer any one of the following:-

4-a. Sketch the CZ process and explain its various parts. Also write its advantages 7

and disadvantages. (CO1)

4-b. Differentiate between: (a) Polycrystalline and a single crystalline material. (b) 7 Intrinsic and extrinsic semiconductors. (CO1)

5. Answer any one of the following:-

5-a.	Sketch and explain vertical and horizontal tube furnace for oxide growth. (CO2)	7	
5-b.	Sketch a neat diagram and explain fabrication process of a NMOS device. (CO2)	7	
6. Answer any <u>one</u> of the following:-			
6-a.	Explain different types of diffusion furnace with suitable diagram. (CO3)	7	
6-b.	Describe Contact Printing related to optical lithography. (CO3)	7	
7. Answer any <u>one</u> of the following:-			
7-a.	Derive expressions for Fick's Second Law of Diffusion. (CO4)	7	
7-b.	Discuss Molecular Beam Epitaxy in detail with diagram. (CO4)	7	
8. Answer any <u>one</u> of the following:-			
8-a.	Explain the various types of Pin -Through – Hole Package with the help of a neat diagram. (CO5)	7	
8-b.	Explain the various steps of CMOS transistor fabrication using n well	7	

8-b. Explain the various steps of CMOS transistor fabrication using n well technique with diagram. (CO5)