Printed Page:- **Subject Code:- AMTVL0102**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech

SEM: I - THEORY EXAMINATION (2022 - 2023)

Subject: Advanced Digital Design using Verilog

Time: 3 Hours **Max. Marks: 70**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* **three Sections -A, B, & C.** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION A **15**

1. Attempt all parts:-

1-a. Which of the following HDLs are IEEE standards? (CO1) 1

(a) VHDL and Verilog

(b) C and C++

(c) Altera and Xilinx

(d) Quartus II and MaxPlus II

1-b. Which versions of the Verilog is known as System Verilog? (CO2) 1

(a) Verilog version 3.0

(b) Verilog version 1.0

(c) Verilog version 1.5

(d) Verilog version 4.0

1-c. In an assignment statement, OUT signal can be used only to the _____. (CO3) 1

(a) Left of <= operator

(b) Right of <= operator

(c) Any side of <= operator

(d) Right of := operator

1-d. Output values of Moore type FSM are determined by its _____. (CO4) 1

(a) Input values

(b) Output values

(c) Clock input

(d) Current state

1-e. The pipelining process is also called as _____. (CO5) 1

(a) Superscalar operation

(b) Assembly line operation

(c) Von Neumann cycle

(d) None of the mentioned

2. Attempt all parts:-

2.a. Is the Verilog a case sensitive language? What do you mean by case sensitive? (CO1) 2

2.b. What do you mean by continuous assignment? (CO2) 2

2.c. What is the difference between the synthesis tasks and functions? (CO3) 2

2.d. Define Ideal MOS switches. (CO4) 2

2.e. What is the role of Cache memory in Pipelining? (CO5) 2

SECTION B **20**

3. Answer any <u>five</u> of the following:-

3-a. Explain top-down design methodology with block diagram and example. (CO1) 4

3-b. Explain in detail different level of abstraction in Verilog. (CO1) 4

3-c. Write Verilog HDL code for 4x1 Multiplexer using gate level modeling. (CO2) 4

3-d. Discuss Excitation table and Clock Diagram for D Flip Flop. Also Write Verilog code for D FF in Data Flow Modeling. (CO2) 4

3.e. Explain synthesis process with a block diagram and all terminologies. (CO3) 4

3.f. Explain Register Banks with diagram. Give a description about Verilog modelling of Register Banks. (CO4) 4

3.g. Discuss Throughput in pipelining. Write down the clocking issue in pipelining. (CO5) 4

SECTION C **35**

4. Answer any <u>one</u> of the following:-

4-a.	Write the note on :i) all Verilog Operators ii) Verilog Datatypes. (CO1)	7
4-b.	Explain the transport and inertial delay. (CO1)	7
5. Answer any <u>one</u> of the following:-		
5-a.	Explain blocking and non-blocking statements with relevant examples. (CO2)	7
5-b.	Implement Full Subtractor circuit using gate level modeling. (CO2)	7
6. Answer any <u>one</u> of the following:-		
6-a.	What is Synthesis? Draw the block diagram for HDL based synthesis with each block explanation. (CO3)	7
6-b.	Write the difference between Pre-Synthesis & Post-synthesis with block diagram and all terminologies. (CO3)	7
7. Answer any <u>one</u> of the following:-		
7-a.	Explain Datapath and control design in Processor. Write down the Verilog code for Modeling Datapath. (CO4)	7
7-b.	Discuss FSM with block diagram. Explain Verilog code for GCD calculation. (CO4)	7
8. Answer any <u>one</u> of the following:-		
8-a.	Write down the stage wise operation in Pipeline. (CO5)	7
8-b.	Difference between RAM and ROM. Design a Single - port RAM with synchronous read/write using Verilog code. (CO5)	7