Printed Page:- **Subject Code:- AMTVL0101**

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NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech

SEM: I - THEORY EXAMINATION (2022 - 2023)

Subject: CMOS Digital VLSI Design

Time: 3 Hours **Max. Marks: 70**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* **three Sections -A, B, & C.** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION A **15**

1. Attempt all parts:-

1-a. What does MOSFET stands for? (CO1) 1

(a) Metal Oxide Semiconductor Field Effect Transistor

(b) Modern Oxidized Silicon based Field Effect Transistor

(c) Modern Oxidized Silicon based Force Effect Transistor

(d) Metal Oxide silicon Field Equivalent Transistor

1-b. When the input of the CMOS inverter is equal to Inverter Threshold Voltage Vth, the transistors are operating in: (CO2) 1

(a) N-MOS is cutoff, p-MOS is in Saturation

(b) P-MOS is cutoff, n-MOS is in Saturation

(c) Both the transistors are in linear region

(d) Both the transistors are in saturation region

1-c. The boolean function Y=AB+CD is to be realized using only 2 input NAND gates. The minimum number of gates required is____. (CO3) 1

(a) 2

(b) 3

(c) 4

(d) 5

1-d. In CMOS domino logic is used --------- (CO4) 1

(a) Two phase clock

(b) Three phase clock

(c) One phase clock

(d) Four phase clock

1-e. Which among the following is used for high density designs for memories. (CO5) 1

(a) DRAM

(b) SRAM

(c) Flip-Flops

(d) Latches

2. Attempt all parts:-

2.a. What do you mean by Channel length modulation? (CO1) 2

2.b. Why static power dissipation is low in CMOS inverter ? (CO2) 2

2.c. Draw CMOS diagram of the function Y=(A.(B+C))' (CO3) 2

2.d. What is precharge evaluate logic in dynamic CMOS logic? (CO4) 2

2.e. Discuss the types of semiconductor memories. (CO5) 2

SECTION B **20**

3. Answer any <u>five</u> of the following:-

3-a. Explain the types of MOSFET capacitances? (CO1) 4

3-b. What are the basic processes involved in fabricating ICs using planar technology? (CO1) 4

3-c. Explain the Delay estimation with different optimization techniques. (CO2) 4

3-d. Describe supply voltage scaling. (CO2) 4

3.e. Explain behaviour of bistable flip flop with the help of a neat diagram. (CO3) 4

3.f. Discuss the classification of Dynamic CMOS logic families. (CO4) 4

3.g. Explain how a bit of information gets stored in SRAM cell? (CO5) 4

SECTION C **35**

4. Answer any <u>one</u> of the following:-

4-a. Explain CMOS n-well process of fabrication with diagram. (CO1) 7

4-b. i) Explain MOS structure in detail and find how and why the inversion layer is formed? (CO1) 7

ii) Differentiate between Enhancement type MOSFET and Depletion Type MOSFET.

5. Answer any <u>one</u> of the following:-

5-a. Write short note on: (CO2) 7

i. Logical Effort

ii. Parasitic Delay.

5-b. Derive the expression for V_{IL}, V_{IH}, V_{th} for CMOS inverter. (CO2) 7

6. Answer any <u>one</u> of the following:-

6-a. Implement the function F=AB+A'C'+AB'C using Transmission gates. (CO3) 7

6-b. Discuss the working of CMOS Master Slave JK FF with the help of a neat diagram. (CO3) 7

7. Answer any <u>one</u> of the following:-

7-a. Explain the working of pass transistor circuit. Also explain how the charge stored affects the transfer of logic “1” and “0” in NMOS pass transistor circuits. (CO4) 7

7-b. Explain voltage bootstrapping with diagram. Construct MOSFET based C_{boot} for Voltage bootstrapping. (CO4) 7

8. Answer any <u>one</u> of the following:-

8-a. Elaborate the sources of leakage current in memories, its causes and remedies. (CO5) 7

8-b. Explain Read and Write operation of 3T DRAM cell with the help of a neat diagram. What do you understand by refresh operation and why it is required? (CO5) 7