Printed Page:- Subject Code:- AMTVL0102

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute)

Affiliated to Dr. A.P.J. Abdul Kalam Technical University, Uttar Pradesh, Lucknow

M.Tech

SEM: I - CARRY OVER THEORY EXAMINATION - AUGUST 2022

Subject: Advanced Digital Design using Verilog

Time: 03:00 Hours Max. Marks: 70

General Instructions:

1. The question paper comprises three sections, A, B, and C. You are expected to answer them as directed.
2. Section A - Question No- 1 is 1 marker & Question No- 2 carries 2 marks each.
3. Section B - Question No-3 is based on external choice carrying 4 marks each.
4. Section C - Questions No. 4-8 are within unit choice questions carrying 7 marks each.
5. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION A 15

1. Attempt all parts:-

1-a. VHSIC stands for _____ (CO1) 1

(a) Very High Speed Integrated Circuits

(b) Very Higher Speed Integration Circuits

(c) Variable High Speed Integrated Circuits

(d) Variable Higher Speed Integration Circuits

1-b. _____ operator usually comes before the operand. (CO2) 1

(a) Unary

(b) Binary

(c) Ternary

(d) None

1 Which of the following is not defined by the entity? (CO3) 1

(a) Direction of any signal

(b) Names of signal

(c) Different ports

(d) Behavior of the signals

1-d. In FSM diagram what does circle represent? (CO4) 1

(a) Change of state

(b) State

(c) Output value

(d) Initial state

1-e. What are the two constructs used in most of the behavioural modelling? (CO5) 1

(a) Assign

(b) Begin and end

(c) Initial and always

(d) Always and end

2. Attempt all parts:-

2-a. Write down the syntax for module block in Verilog. (CO1) 2

2-b. What is wait statement? (CO2) 2

2-c. What is The Difference Between Sequential Circuit and Combinational Circuit? (CO3) 2

2-d. Write down the conditions required for the synthesis of combinational circuit. (CO4) 2

2-e. Explain Data hazards. (CO5) 2

SECTION B 20

3. Answer any five of the following:-

3-a. What are the advantages of HDLs compared to traditional schematic based design? (CO1) 4

3-b. What are the needs and basic features of HDL? (CO1) 4

3-c. Explain structured procedure statements in Verilog. (CO2) 4

3-d. Write Verilog HDL code for 4x1 Multiplexer using gate level modeling. (CO2) 4

3 Write Verilog dataflow description of 1 Bit full adder. (CO3) 4

3 Explain Bit Slicing. (CO4) 4

3-g. Write down the difference between Linear and Non-Linear Pipeline. (CO5) 4

SECTION C 35

4. Answer any one of the following:-

4-a. Explain the declaration of constants, variables and signals in Verilog with example. (CO1) 7

4-b. Explain the transport and inertial delay. (CO1) 7

5. Answer any one of the following:-

5-a.	Explain blocking and non-blocking statements with relevant examples. (CO2)	7
5-b.	Write Verilog HDL code for 4-bit Up-Down Counter. (CO2)	7

6. Answer any one of the following:-

6-a.	Explain verilog primitives in detail. (CO3)	7
6-b.	Write a verilog code for priority encoder using Verilog and explain with a neat block diagram. (CO3)	7

7. Answer any one of the following:-

7-a.	Explain in detail about Finite State Machine. (CO4)	7
7-b.	Explain in detail about Modeling modules of Datapath. (CO4)	7

8. Answer any one of the following:-

8-a.	Design a Verilog code for clocking issue in Pipeline. (CO5)	7
8-b.	Write down the stage wise operation in Pipeline. (CO5)	7