Printed Page:- Subject Code:- AMTCSE0216

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

M.Tech.

SEM: II - THEORY EXAMINATION (2021 - 2022)

Subject: Advanced Computer Architecture

Time: 3 Hours Max. Marks: 70

General Instructions:

1. The question paper comprises three sections, A, B, and C. You are expected to answer them as directed.
2. Section A - Question No- 1 is 1 marker & Question No- 2 carries 2 marks each.
3. Section B - Question No-3 is based on external choice carrying 4 marks each.
4. Section C - Questions No. 4-8 are within unit choice questions carrying 7 marks each.
5. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION A 15

1. Attempt all parts:-

1-a. The three control signals used in the mechanism of Bus Arbitration are:- (CO1) 1

(a) Bus Busy, Bus Grant and Bus Request

(b) Bus Busy, Bus Acknowledge and Bus Grant

(c) Bus Active, Bus Busy and Bus Grant

(d) Bus Acknowledge, Bus Active and Bus Grant

1-b. Basic task for control unit is (CO2) 1

(a) Sequencing

(b) execution

(c) both a & b

(d) none of the above

1-c. Which of the following is not a Pipeline Conflicts? (CO3) 1

(a) Timing Variations

(b) Branching

(c) Load Balancing

(d) Data Dependency

1-d. VLIW stands for _____ (CO4) 1

(a) very long instruction word

(b) very long instruction width

(c) very large instruction word

(d) None of the above

1-e. Basic difference between vector and array processor is (CO5) 1

(a) pipelining

(b) interconnection network

(c) register

(d) None of these

2. Attempt all parts:-

2.a. What is the purpose of Data bus and Address bus? (CO1) 2

2.b. Give microoperations for Increment and skip if zero(ISZ). (CO2) 2

2.c. How hazards can be avoided in pipelining? (CO3) 2

2.d. Define Hit ratio in Memory Access operations. (CO4) 2

2.e. List two advantages of using SIMD computers. (CO5) 2

SECTION B 20

3. Answer any five of the following:-

3-a. A digital computer has a common bus system for 16 register of 32 bits each. The bus is constructed with multiplexers. 4

(i) How many selection inputs are there in each multiplexer?

(ii) What sizes of multiplexers are needed?

(iii) How many multiplexers are there in the bus? (CO1)

3-b. Describe Daisy chaining method with suitable diagram. (CO1) 4

3-c. Differentiate between direct and indirect addressing. (CO2) 4

3-d. Discuss instruction cycle in brief with a suitable diagram. (CO2) 4

3.e. Discuss Clocking and Timing control in a linear pipeline processor. (CO3) 4

3.f. Differentiate between RISC and CISC. (CO4) 4

3.g. Discuss any two vector access memory schemes. (CO5) 4

SECTION C 35

4. Answer any one of the following:-

4-a.	Using Stacks evaluate the following arithmetic expression: 8*7 + 5/6. (CO1)	7
4-b.	Compare the daisy chaining method with polling method in bus arbitration with the help of suitable diagrams. (CO1)	7

5. Answer any one of the following:-

5-a.	Explain how control signals are generated using micro-programmed control. (CO2)	7
5-b.	Write short notes on a) LDA b) STA (CO2)	7

6. Answer any one of the following:-

6-a.	Describe hazard avoidance in pipelining. (CO3)	7
6-b.	Write short notes on a) Throughput b) Clock skewing (CO3)	7

7. Answer any one of the following:-

7-a.	Explain the architecture of superscalar RISC processor in detail. (CO4)	7
7-b.	Differentiate between Paged memory and segmented memory. (CO4)	7

8. Answer any one of the following:-

8	Explain the SIMD programming principles with a suitable diagram. (CO5)	7
8	Explain any one method to implement PRAM model and discuss the pros and cons of that method. (CO5)	7