NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA
(An Autonomous Institute)
Affiliated to Dr. A.P.J. Abdul Kalam Technical University, Uttar Pradesh, Lucknow
M.Tech
SEM: I - THEORY EXAMINATION (2021 - 2022)
Subject: CMOS Digital VLSI Design

Time: 03:00 Hours   Max. Marks: 70

General Instructions:

1. All questions are compulsory. It comprises of three Sections A, B and C.

- Section A - Question No- 1 is objective type question carrying 1 mark each & Question No- 2 is very short type questions carrying 2 marks each.
- Section B - Question No- 3 is Long answer type - I questions carrying 4 marks each.
- Section C - Question No- 4 to 8 are Long answer type - II questions carrying 7 marks each.
- No sheet should be left blank. Any written material after a Blank sheet will not be evaluated/checked.

SECTION A   15

1. Attempt all parts:-

1-a.   The enhancement type basically termed as normally-OFF N MOSFET works only with _____. (CO1)   1
   1. large positive gate voltage
   2. large negative gate voltage
   3. large positive drain voltage
   4. . large negative drain voltage

1-b.   In CMOS fabrication, nMOS and pMOS are integrated in same substrate. (CO2)   1
   1. a) true
   2. b) false

1-c.   The boolean function Y=AB+CD is to be realized using only 2 input NAND gates. The minimum number of gates required is____. (CO3)   1
   1. 2
   2. 3
   3. 4
   4. 5

1-d.   In precharge phase, when capacitor is fully charge it becomes equal to V_{DD}. (T/F) (CO4)   1
   1. TRUE
   2. FALSE

1-e.   Which of the following memories uses one transistor and one capacitor as basic memory unit (CO5)   1
   1. SRAM
   2. DRAM
   3. Both
   4. None

2. Attempt all parts:-

2-a.   Explain the three regions of operation of a MOSFET. (CO1)   2

2-b.   Compare between CMOS and bipolar technologies. (CO2)   2

2-c.	Draw CMOS diagram of the function Y=(A.(B+C))' (CO3)	2
2-d.	What is pass transistor? (CO4)	2
2-e.	Differentiate between SRAM and DRAM. (CO5)	2

<div align="center">SECTION B   20</div>

3. Answer any <u>five</u> of the following:-

3-a.	Explain the energy band diagram for combined MOS system and elaborate why there is bending near the oxide semiconductor interface? (CO1)	4
3-b.	Explain accumulation, depletion, inversion regions of operation in case externally biased MOS structure.(CO1)	4
3-c.	Explain briefly the scaling in VLSI. (CO2)	4
3-d.	What is switching power dissipation of CMOS inverter? (CO2)	4
3-e.	Draw CMOS diagram of the function Y=(A.B+C). (D+E))' (CO3)	4
3-f.	Explain synchronous dynamic circuit techniques with neat diagrams.(CO4)	4
3-g.	What is DRAM ? Explain DRAM with the diagram.(CO5)	4

<div align="center">SECTION C   35</div>

4. Answer any <u>one</u> of the following:-

| 4-a. | What is channel length modulation? Calculate effective channel length and new drain current.(CO1) | 7 |
| 4-b. | Define Noise immunity and Noise margins. Calculate VOH, VOL, VIL, VIH for a depletion-load nMOS Inverter. Explain why we don't use enhancement-load nMOS inverter? (CO1) | 7 |

5. Answer any <u>one</u> of the following:-

| 5-a. | What is CMOS inverter? Draw the voltage transfer curve (VTC) and explain. (CO2) | 7 |
| 5-b. | What is threshold voltage for CMOS inverter? Calculate Noise margin for CMOS inverter. (CO2) | 7 |

6. Answer any <u>one</u> of the following:-

| 6-a. | Explain the design of CMOS Full Adder with the help of a neat diagram. (CO3) | 7 |
| 6-b. | Draw and explain the D FF design with the help of transmission gate. (CO3) | 7 |

7. Answer any <u>one</u> of the following:-

| 7-a. | What is dynamic CMOS transmission gate logic? Explain it with two different stages and also explain the working of soft node. (CO4) | 7 |
| 7-b. | Differentiate between synchronous and asynchronous sequential circuits? What are the synchronous dynamic circuit techniques? (CO4) | 7 |

8. Answer any <u>one</u> of the following:-

| 8-a. | Distinguish between NOR flash memory cell and NAND flash memory cell. (CO5) | 7 |
| 8-b. | What do you mean by static RAM. Explain the Read and Write operations of 6 Transistor SRAM cell with a neat diagram. (CO5) | 7 |