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NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute)

Affiliated to Dr. A.P.J. Abdul Kalam Technical University, Uttar Pradesh, Lucknow

M.Tech

FIRST YEAR (SEMESTER-II) THEORY EXAMINATION (2020-2021)

(Objective Type)

Subject Code: AMTCSE0216 **Max. Mks. : 40**

Subject: Advanced Computer Architecture **Time : 70 Minutes**

General Instructions:

All questions are compulsory.

Question No- 1 to 5 are objective type question carrying 2 marks each.

Question No- 6 to 20 are also objective type/Glossary based question carrying 2 marks each.

Q.No	Question Content	Question Image	Category	Sub Category	Marks	Options Randomization	Type	Difficulty	Correct	Option1	Option2	Option3	Option4
1	A digital circuit that generates single output by taking multiple inputs		Single Choice Questions	Single Choice Questions	2		Single Choice	Smart	Multiplexer	Multiplexer	Decoder	Adder	Demultiplexer
2	The instruction “JUMP” belongs to		Single Choice Questions	Single Choice Questions	2		Single Choice	Smart	control transfer & branch instructions	sequential control flow instructions	control transfer instructions	branch instructions	control transfer & branch instructions
3	The performance of a pipelined processor suffers if		Single Choice Questions	Single Choice Questions	2		Single Choice	Smart	All of the above	The pipeline stages have different delays	Consecutive instructions depend on each other	The pipeline stages share single hardware resources	All of the above
4	VLIW stands for _____		Single Choice Questions	Single Choice Questions	2		Single Choice	Smart	very long instruction word	very long instruction word	very long instruction width	very large instruction word	None of the above
5	Which of the following operations in instruction pipeline processing is performed first?		Single Choice Questions	Single Choice Questions	2		Single Choice	Smart	Fetch instruction	Calculate operand address	Fetch instruction	Decode instruction	Execute instruction
6	Each stage in pipelining should be completed within _____ cycle.		Glossary I	Glossary I	2		Single Choice	Smart	1	pipelining	1	to convert sequential scalar instructions into vector instructions	
7	Basic difference between vector and array processor is		Glossary I	Glossary I	2		Single Choice	Smart	pipelining	pipelining	1	to convert sequential scalar instructions into vector instructions	
8	The task of vectorizing compiler is		Glossary I	Glossary I	2		Single Choice	Smart	to convert sequential scalar instructions into vector instructions	pipelining	1	to convert sequential scalar instructions into vector instructions	
9	The Sun micro systems processors usually follow _____ architecture		Glossary II	Glossary II	2		Single Choice	Smart	RISC	Physical addresses	RISC	Complex instruction set computer	
10	_____ is stored in a Translation Look aside Buffer		Glossary II	Glossary II	2		Single Choice	Smart	Physical addresses	Physical addresses	RISC	Complex instruction set computer	
11	___ consists of a variety of expert instruction and may just not be frequently used in practical programs.		Glossary II	Glossary II	2		Single Choice	Smart	Complex instruction set computer	Physical addresses	RISC	Complex instruction set computer	
12	The presence of anti dependencies and output dependencies leads to		Glossary III	Glossary III	2		Single Choice	Smart	WAR and WAW stalls	Committed	WAR and WAW stalls	1967	
13	When an instruction is guaranteed to complete, it is called		Glossary III	Glossary III	2		Single Choice	Smart	Committed	Committed	WAR and WAW stalls	1967	
14	The Tomasulo algorithm is a hardware algorithm developed in		Glossary III	Glossary III	2		Single Choice	Smart	1967	Committed	WAR and WAW stalls	1967	

Q.No	Question Content	Question Image	Category	Sub Category	Marks	Options Randomization	Type	Difficulty	Correct	Option1	Option2	Option3	Option4
15	The Control unit of a computer generates _____ for execution of instruction		Glossary IV	Glossary IV	2		Single Choice	Smart	Control signals	Micro-operations	Control signals	Microinstructions	
16	Microprogram consisting of _____ is stored in control memory of control unit		Glossary IV	Glossary IV	2		Single Choice	Smart	Microinstructions	Micro-operations	Control signals	Microinstructions	
17	To execute machine instruction, a set of _____ in a proper sequence must be performed		Glossary IV	Glossary IV	2		Single Choice	Smart	Micro-operations	Micro-operations	Control signals	Microinstructions	
18	A collection of lines that connects several devices is called		Glossary V	Glossary V	2		Single Choice	Smart	Bus	bus arbitration	4	Bus	
19	To resolve the clash over the access of the system bus, we use		Glossary V	Glossary V	2		Single Choice	Smart	bus arbitration	bus arbitration	4	Bus	
20	selection lines are there in common bus for 16 registers of 16 bits each.		Glossary V	Glossary V	2		Single Choice	Smart	4	bus arbitration	4	Bus	