NOIDA INSTITUTE OF ENGG. & TECHNOLOGY, GREATER NOIDA, GAUTAM BUDDH NAGAR
(AN AUTONOMOUS INSTITUTE)

Affiliated to

DR. A.P.J. ABDUL KALAM TECHNICAL UNIVERSITY UTTAR PRADESH, LUCKNOW

Evaluation Scheme & Syllabus

For

Minor Degree / Specialization

in

VLSI Design

School of Electronics & Communication Engineering

(Effective from the Session: 2022-23)

NOIDA INSTITUTE OF ENGG. & TECHNOLOGY, GREATER NOIDA, GAUTAM BUDDH NAGAR
(AN AUTONOMOUS INSTITUTE)

Minor Degree / Specialization
VLSI Design

EVALUATION SCHEME

Sl. No.	Subject Codes	Subject Name	Periods			Evaluation Scheme				End Semester		Total	Credit	SEM
			L	T	P	AA	QZ	TOTAL	PS	TE	PE			
1	AMSVL0301	Digital Integrated Circuit	3	0	0	25	25	50		100		150	3	III
2	AMSVL0401	Advanced Digital Design	3	0	0	25	25	50		100		150	3	IV
3	AMSVL0501	Digital Logic Design Using VHDL and Verilog	3	0	0	25	25	50		100		150	3	V
4	AMSVL0601	Programming Fundamentals for Design and Verification	3	0	0	25	25	50		100		150	3	VI
5	AMSVL0701	VLSI Testing and Testability	3	0	0	25	25	50		100		150	3	VII
6	AMSVL0351	Digital Integrated Circuit Lab	0	0	2				25		25	50	1	III
7	AMSVL0451	Advanced Digital Design Lab	0	0	2				25		25	50	1	IV
8	AMSVL0551	Digital Logic Design Using VHDL and Verilog Lab	0	0	2				25		25	50	1	V
9	AMSVL0751	Capstone Project	0	0	2				50		50	100	2	VII
		GRAND TOTAL										1000	20	

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Branch wise Minor Degree / Specialization Details

S.no.	Name of Minor Degree/Specialization	Streams/Branches of B.Tech. Programs whose students are eligible to opt for the Minor Degree	Streams/Branches of B.Tech. Programs whose students are eligible to opt for the Specialization
1	Artificial Intelligence and Machine Learning	All Branches except CSE and EC related Branches	CSE and EC related Branches
2	Data Science	All Branches except CSE and EC related Branches	CSE and EC related Branches
3	E-mobility	All Branches except ME related Branches	Only ME Branch
4	VLSI Design	All Branches except EC related Branches	Only EC Branch

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Guidelines for assessment of Minor Degree / Specialization Program

For Theory Paper

Internal (50)		External (100)
AA (25)	QZ(25)	
5 Assignments of 5 marks each	5 Quiz papers of 5 marks each	Theory Examination will be Conduct at the end of Semester

For Practical Paper

Internal (25)	External (25)
On the basis of continuous Assessment	Practical Examination will be Conduct at the end of Semester

Course Code	AMSVL0301	L T P	credits
Course Title	Digital Integrated Circuit	3 0 0	3

Course Objective: Students will learn about

1	MOS and CMOS logic gate design.
2	CMOS Combinational and Sequential logic circuit design
3	Dynamic logic circuit Design
4	VLSI design methodology
5	Different ASIC Design Flow

Pre-requisites: Basic knowledge of MOSFET and Digital Electronics

Course Contents/Syllabus

UNIT-I	MOSFET and CMOS Theory	8 hours

Evolution of VLSI, MOS threshold voltage, MOS device design equations, MOSFET scaling and small geometry effects, MOSFET capacitances.
CMOS logic gate design: CMOS inverter, DC characteristics, rise time, fall time delays, noise margin, static & dynamic power dissipation, CMOS NAND, NOR, XOR and XNOR gates, Transistor sizing.

UNIT-II	CMOS Combinational and Sequential logic circuit design	8 hours

CMOS Combinational Circuit: Design Half Adder, Full Adder, Multiplexer, Demultiplexers using CMOS.

CMOS Sequential logic circuits: Design SR latch, SR flip flop, JK flip flop, D flip flop using CMOS.

UNIT-III	Dynamic logic circuit Design	8 hours

Logic Gate design using pass transistor, different Combinational Circuit design using transmission gate and Pseudo NMOS logic.

Dynamic logic circuits: Basic principle, non-ideal effects, domino CMOS logic, high performance dynamic CMOS circuits, clocking issues, clock distribution.

UNIT IV	VLSI Design Methodology	8 hours

VLSI design methodology, design Hierarchy, concept of regularity, modularity & locality, VLSI design style like Full Custom, Semi-Custom, Gate Array, Standard Cell and FPGA, design flow, Design quality Parameters, computer aided design technology, stick diagram and design rules, lambda-based design rules.

UNIT-V	ASIC Design Flow	8 hours

Introduction of Application Specific Integrated Circuit (ASIC) Design Flow: An overview of Backend VLSI Design Flow – Libraries, Floor-planning, Placement, Routing, Verification, Testing. Specifications and Schematic cell Design, Spice simulation Analysis of analog and digital circuits, Circuit Extraction, Electrical rule check, Layout Vs. Schematic (LVS), Post-layout Simulation and Parasitic extraction, Design format, Timing analysis, Back notation and Post layout simulation, ASIC design implementation.

Course Outcomes: After completion of this course students will be able to

CO 1	Express the concept of MOS design and CMOS logic gate design.	K1, K2
CO 2	Design CMOS Combinational and Sequential logic circuit.	K1, K2, K3
CO 3	Implement various logic gate using Dynamic logic Technique.	K1, K2, K3
CO 4	Discuss the VLSI design methodology and its design flow.	K1, K2

CO 5	Describe ASIC Design Flow.	K1, K2, K3

Text Books:

1. Sung-Mo Kang & Yosuf Leblebici, "CMOS Digital Integrated Circuits: Analysis & Design",Mcgraw Hill, 4th Edition.
2. A.S. Sedra and K.C. Smith, "Microelectronic Circuits," Saunder's College11 Publishing, 4th edition.

Reference Books:

1. Introduction to VLSI, Eshraghian & Pucknell, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2007
2. W.Wolf, Modern VLSI Design: System on Chip, Third Edition, Pearson, 2002.

Unit 1	https://www.youtube.com/watch?v=MuBiC9yz2fc https://www.youtube.com/watch?v=fqiYu6IOtmU&t=2225s https://www.youtube.com/watch?v=m5rEKAqHyKo&t=1707s
Unit 2	https://www.youtube.com/watch?v=8caQpnxa3iE https://www.youtube.com/watch?v=RZo--xYfTR4&t=1232s https://www.youtube.com/watch?v=jhEMjTG20tI https://www.youtube.com/watch?v=A8qOlc-jLIA
Unit 3	https://www.youtube.com/watch?v=q8adOpQx7tc&t=2187s https://www.youtube.com/watch?v=Eu9MLCekmwU https://www.youtube.com/watch?v=u-s5PL-qbZA
Unit 4	https://www.youtube.com/watch?v=20nvQRVwz0&list=PLCmoXVuSEVHlEJi3SwdyJ4EICffuyqpjk&index=3 https://www.youtube.com/watch?v=7mAL0Au02To&list=PLCmoXVuSEVHlEJi3SwdyJ4EICffuyqpjk&index=4
Unit 5	https://www.youtube.com/watch?v=oZSv68esbgI&t=22s https://www.youtube.com/watch?v=4cPkr1VHu7Q&t=8s

Course Code	AMSVL0401	L T P	Credit
Course Title	Advanced Digital Design	3 0 0	03

Course Objective:

1	To study finite state machines and its realization.
2	To study asynchronous Sequential machine.
3	To learn Designing of Digital logic using PLD.
4	To get knowledge of different FPGA series.
5	To study different CPLD series.

Pre-requisites: Basics of CMOS and Digital Electronics.

Course Contents / Syllabus

UNIT-I	**Finite State Machine (FSM)**	8 hours

Introduction, Design Strategies, Mealy & Moore model, Realization of State Diagram & state table from verbal description, Minimization of State Table from completely & Incompletely specified State Machine, Introduction to Algorithmic State Machine.

UNIT-II	**Asynchronous Sequential Circuit**	8 hours

Introduction to Asynchronous Sequential Machine (ASM), fundamental & pulse mode Asynchronous Sequential machine, Secondary State Assignments in Asynchronous Sequential machine, Races & Hazards.

UNIT-III	**Programmable Logic Devices (PLD)**	8 hours

Introduction, Architecture, Features & Digital Design of ROM, EPROM, EEPROM, Flash Memory, PLA, PAL & PGA.
Design of Combinational and Sequential Circuits, keypad scanner using PLD.

UNIT-IV	**Field Programmable Gate Array (FPGA)**	8 hours

FPGA-Configurable Logic Block, IO block programmable interconnect, LUT based, Multiplexer based Technology mapping, Routing architecture, FPGA Design flow.
Block Diagram and CLB of Xilinx FPGA XC3000 and Xilinx FPGA XC4000, use of One-hot Assignment Technique in FPGA.

UNIT-V	**Complex Programmable Logic Devices (CPLD)**	8 hours

Difference between FPGA and CPLDs, Altera series – Max 5000/7000 series and Altera FLEX logic- 10000 series CPLDs, AMD's- CPLD (Mach 1 to 5), Cypress FLASH 370 Device technology, Lattice plsi architectures – 3000 series – Speed performance and system programmability.

Course Outcome: After completion of this course students will be able to

CO 1	Realize Finite State Machines.
CO 2	Formulate Asynchronous Sequential Machine.
CO 3	Design Digital logic using PLD.
CO 4	Explain different FPGA series.
CO 5	Explain different CPLD series.

Text books:

1. P. K. Chan& S. Mourad, Digital Design using Field Programmable Gate Array, Prentice Hall.
2. Charles H Roth, Jr., “Digital Systems Design Using VHDL”, PWS, 1998.
3. S. Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Pub.
Reference Books:
1. J. Old Field, R. Dorf, Field Programmable Gate Arrays, John Wiley& Sons, Newyork.
2. S.Brown,R.Francis, J.Rose, Z.Vransic, Field Programmable GateArray,Kluwer Pub.
3. Richard FJinder , “Engineering Digital Design,”Academic press

Unit-1	Mealy & Moore model,	https://www.youtube.com/watch?v=O3If0Nr9to0 (NPTEL) https://www.youtube.com/watch?v=_88FzOc9GzA https://www.youtube.com/watch?v=_gazATZF0R8
	Realization of State Diagram & state table from verbal description,	https://www.youtube.com/watch?v=NNOSWnTHakY https://www.youtube.com/watch?v=IXORIs1dHs0
	Minimization of State Table from completely & Incompletely specified State Machine	https://www.youtube.com/watch?v=2JDLqfYmhDk https://www.youtube.com/watch?v=XBIV1Gz3J-w
	Introduction to Algorithmic State Machine.	https://www.youtube.com/watch?v=vYUoYmtpg_E https://www.youtube.com/watch?v=7GJvH1EQCX4
Unit-2	Introduction to Asynchronous Sequential Machine (ASM)	https://www.youtube.com/watch?v=nsPhvW16lek &list=PLbRMhDVUMngfV8C6ElNAUaQQz06wEhFM5&index=54
	fundamental & pulse mode Asynchronous Sequential machine	https://www.youtube.com/watch?v=nsPhvW16lek
	Secondary State Assignments in Asynchronous	https://www.youtube.com/watch?v=PdY0yDMC2pg

	Sequential machine	
	Races & Hazards.	https://www.youtube.com/watch?v=PdY0yDMC2pg https://www.youtube.com/watch?v=pzhAkdh1UO8
Unit-3	Introduction, Architecture, Features & Digital Design of ROM, EPROM, EEPROM, Flash Memory	https://www.youtube.com/watch?v=tas2eUavhRE
	PLA, PAL & PGA	https://www.youtube.com/watch?v=gCAYY0fHPq4 https://www.youtube.com/watch?v=qlq4NHk5Y_w https://www.youtube.com/watch?v=lAqERUtAsqk https://www.youtube.com/watch?v=VW29K1jGLnk https://www.youtube.com/watch?v=BhSWeGzRqEc https://www.youtube.com/watch?v=BMq6ohsBDpc https://www.youtube.com/watch?v=RNLtpp2ZHbE
	Design of Combinational and Sequential Circuits, keypad scanner using PLD.	https://www.youtube.com/watch?v=8-LpYxLLTr8 https://www.youtube.com/watch?v=SzV4l0_1MCQ https://www.youtube.com/watch?v=XaJF2OYzjLI&list=PLbMVogVj5nJSY-1XxFHgwgtj2F7mB7NuV&index=33
Unit-4	FPGA-Configurable Logic Block, IO block programmable interconnect, LUT based,	https://www.youtube.com/watch?v=gUsHwi4M4xE&list=RDQMvKBuISMkoYE&start_radio=1 (What Is An FPGA?) https://www.youtube.com/watch?v=jbOjWp4C3V4 (FPGA Architecture)
	Multiplexer based Technology mapping, Routing architecture, FPGA Design flow.	https://www.youtube.com/watch?v=jbOjWp4C3V4 https://www.youtube.com/watch?v=C8Bp1UH9D8E https://www.youtube.com/watch?v=yG3dBx8kToM https://www.youtube.com/watch?v=RnXK0n0grmc

	Block Diagram and CLB of Xilinx FPGA XC3000 and Xilinx FPGA XC4000	https://www.youtube.com/watch?v=8RJyie0eXS0 (Xilinx XC 3000 Séries) https://www.youtube.com/watch?v=WKGY7Y9wJvw (Xilinx XC 4000 Séries)
	use of One-hot Assignment Technique in FPGA.	https://www.youtube.com/watch?v=T2b5wlBcE-E https://www.youtube.com/watch?v=Aj2a_AkyXcE
Unit-5	Difference between FPGA and CPLDs,	https://www.youtube.com/watch?v=jbOjWp4C3V4 (FPGA Architecture)
	Altera series – Max 5000/7000 series and Altera FLEX logic-10000 series CPLDs,	https://www.youtube.com/watch?v=VE3jdCxzTjU (AlteraMax7000, AltraFLEX10k) https://www.youtube.com/watch?v=oDwBWvUxOrU (Configuration Schemes for Intel® FPGAs) https://www.youtube.com/watch?v=OuO84HeLqDo&list=PLbMVogVj5nJSY-1XxFHgwgtj2F7mB7NuV&index=41 (Altera & Actel FPGAs) https://www.youtube.com/watch?v=OuO84HeLqDo&list=PLbMVogVj5nJSY-1XxFHgwgtj2F7mB7NuV&index=42 https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ds/archives/m5000.pdf https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ds/archives/m7000.pdf
	AMD's- CPLD (Mach 1 to 5)	
	Cypress FLASH 370 Device technology	https://www.youtube.com/watch?v=5qkHodxUxNU
	Lattice plsi architectures – 3000 series – Speed performance and system programmability.	https://www.datasheetarchive.com/pdf/download.php?id=d5c50524830e8cf8efe8301f01f66f580ee996&type=P&term=LATTICE%2520plsi%2520architecture%25203000%2520SERIES https://www.datasheetarchive.com/pdf/download.php?id=796cc460d3dae1bafb535546728a4b6004f1ef&type=P&term=LATTICE%2520plsi%2520architecture%25203000%2520SERIES

Course Code	AMSVL0501	L T P	Credits
Course Title	Digital Logic Design Using VHDL and Verilog	3 0 0	3

Course Objective: The student will	
1	Understand the basic knowledge of VHDL.
2	Able to identify VHDL Modelling Types
3	Learn about Combinational modules and Sequential modules using VHDL
4	Learn about Verilog HDL Fundamentals.
5	Design Verilog Combinational & Sequential Circuits modules.

Pre-requisites: Digital logic Design.

Course Contents/Syllabus

UNIT-I	Introduction to VHDL	8 hours

Need of VHDL, HDL Design Flow, Basic language element of VHDL, Port Type, Configurational Declaration, Package Declaration, Package body, Data Objects, Data Types, Subprograms.

UNIT-II	VHDL Modeling Types & VHDL Combinational Circuits modules	8 hours

Behavioural modelling: variable and signal assignment Statements.
Data flow modelling: concurrent and conditional signal assignment statement.
Structural modelling: component declaration and component instantiation.

VHDL code for Logic gates, Decoder, Encoder, Multiplexers and Demultiplexers.
Standard combinational modules: Adder modules- Design of full-adder module and a Carry-look ahead Adder module.

UNIT-III	Sequential modules using VHDL	8 hours

VHDL code for SR,JK,D,T Flip Flop, Standard sequential modules: Register Module, Shift register module, counter module.

UNIT- IV	Introduction to Verilog	8 hours

Basic language element of Verilog, Behavioural modelling, Data flow modelling, Structural modelling, Switch Level modelling, Differences between tasks and functions, Procedural continuous assignments, overriding parameters, conditional compilation and execution, Verilog code for basic logic gates.

UNIT-V	Verilog Combinational & Sequential Circuits modules	8 hours

Verilog code for Decoder, Encoder, Multiplexers and Demultiplexers.
Standard combinational modules: Adder modules- Design of full-adder module and a Carry-look ahead Adder module.
Verilog code for SR, JK, D, T Flip Flop, Standard sequential modules: Register Module, Shift register module, counter module, Modelling Finite State Machines(FSM) with Verilog.

Course Outcomes: After completion of this course students will be able to

CO 1	Know the basic building block of VHDL.	K1,K2
CO 2	Outline various VHDL Modeling styles.	K2
CO 3	Program standard combinational modules using VHDL.	K4,K6
CO 4	Program standard sequential modules using VHDL.	K4,K5
CO 5	Know the basic concept of Verilog.	K1,K3

Text Books:		
1. J. Bhaskar, " A VHDL Primer", Addison Wesley, 1999.		
2. Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis, Second Edition", Prentice Hall PTR,2003		
3. C. H. Roth, "Digital System Design using VHDL", PWS Publishing		
Reference Books		
1. J.F. Wakerly, "Digital Design-Principles and Practices", PHL		
2. Douglas Perry, "VHDL", MGH		
3. Michae John Sebastian Smith, "Application-Specific Integrated Circuits", Addison- Wesley.		
4. Z. Navabi, " VHDL-Analysis and Modeling of Digital Systems", MGH		
Video Links		
Unit-1	Need of VHDL	https://www.youtube.com/watch?v=eGhgz0tQznc
	HDL Design Flow	https://www.youtube.com/watch?v=lHjGVuc8pvQ
	Basic language element of VHDL	https://www.youtube.com/watch?v=uaGugWIk_Uk
	Port Type	https://www.youtube.com/watch?v=ygCAA2aSaoY
	Configurational Declaration	https://www.youtube.com/watch?v=jZGS1TmRc2s
	Package Declaration	https://www.youtube.com/watch?v=B7cI22riYYw
	Package body	https://www.youtube.com/watch?v=CE-BWT-h0_8
	Data Objects	https://www.youtube.com/watch?v=0rP_idtkn-g
	Data Types	https://www.youtube.com/watch?v=2GZa26T_lvI
	Subprograms	https://www.youtube.com/watch?v=jpTiDSord94
Unit-2	Behavioural modelling: variable and signal assignment Statements.	https://www.youtube.com/watch?v=2M8cN9NCZBU
	Data flow modelling: concurrent and conditional signal assignment statement.	https://www.youtube.com/watch?v=FXqhtAz8nzY
	Structural modelling: component declaration and component instantiation.	https://www.youtube.com/watch?v=YQVRnyrdQxY

	VHDL code for Logic gates,	https://www.youtube.com/watch?v=pD6g661kv_s
	VHDL code for Decoder, Encoder	
	VHDL code for Multiplexers and Demultiplexers	https://www.youtube.com/watch?v=LxKjjet00BI
	Standard combinational modules: Adder modules	https://www.youtube.com/watch?v=fXrbYMDevDU
	Design of full-adder module and a Carry look ahead Adder module	https://www.youtube.com/watch?v=zQYfr5yuPE4
Unit-3	VHDL code for SR Flip Flop	https://www.youtube.com/watch?v=Ek6Dsi3YNTA
	VHDL code for JK Flip Flop	https://www.youtube.com/watch?v=exi4QZ1iW2A
	VHDL code for D Flip Flop	https://www.youtube.com/watch?v=os_qhF4upOQ
	VHDL code for T Flip Flop	https://www.youtube.com/watch?v=_UIyWK_FQOk
	Standard sequential modules: Register Module, Shift Register module	https://www.youtube.com/watch?v=XkBAFhYBauo
	Counter module	https://www.youtube.com/watch?v=nASo9_FyCMg
Unit-4	Basic language element of Verilog	https://www.youtube.com/watch?v=fgyZH98o1rc
	Behavioural modelling	https://www.youtube.com/watch?v=KgSO06yKIJo
	Data flow modelling	https://www.youtube.com/watch?v=Bmxl0bk-W_c
	Structural modelling	https://www.youtube.com/watch?v=Zk2mCKowUt4
	Switch Level modelling	https://www.youtube.com/watch?v=_kDyXCkyCzA
	Differences between tasks and functions	https://www.youtube.com/watch?v=vwvIv43IZ6o

	continuous assignments, overriding parameters, conditional compilation and execution, Procedural	https://www.youtube.com/watch?v=NIaoRQ5U9b0
	Verilog code for basic logic gates	https://www.youtube.com/watch?v=1a2cZDFHJSY
Unit-5	Verilog code for Decoder	https://www.youtube.com/watch?v=5kUOerxLbOc
	Verilog code for Encoder	https://www.youtube.com/watch?v=Uj87Zh2K5ok
	Verilog code for Multiplexers	https://www.youtube.com/watch?v=8Z96GEWNaZI
	Verilog code for Demultiplexers	https://www.youtube.com/watch?v=SzipzVCIDOU
	Standard combinational modules: Adder modules- Design of full-adder module and a Carry-look ahead Adder module	https://www.youtube.com/watch?v=ia4c2SVGYOE

Course Code	AMSVL0601	L T P	Credits
Course Title	Programming Fundamentals for Design and Verification	3 0 0	3

Course Objective: The student will able to learn	
1	C and C++ Programming Fundamentals.
2	HDL Simulation and Synthesis
3	System Verilog Fundamentals
4	System Verilog Design and Interfacing
5	Verification and its Concepts

Pre-requisites: CMOS VLSI Design, Digital logic Design.

Course Contents/ Syllabus

UNIT-I	C and C++ Programming Fundamentals	8 hours

Introduction to C, Data Types and variables, Arrays, Pointers, Functions, Loop, Strings, Structures, Nesting Structures, Array of Structures & Unions.
Introduction to C++, Classes & Objects, Inheritance, Class and Function Templates, Exception Handling, Namespaces.

UNIT-II	HDL Simulation and Synthesis	8 hours

HDL Flow, The concept of Simulation, Types of simulation, HDL Simulation and Modeling, Simulation Vs Synthesis result, The Synthesis Concept, Synthesis of high level constructs, Timing Analysis of Logic circuits, Clock Skew, Clock Jitter, Combinatorial Logic Synthesis, State machine synthesis, Efficient coding styles, Partitioning for synthesis, Pipelining, Resource sharing, Optimizing arithmetic expressions, The Simulation and Synthesis Tools.

UNIT-III	System Verilog	8 hours

Origins, Overview, Need and Importance, System Verilog Declaration Spaces, Data types, System Verilog Literal Values and Built-in Data Types, System Verilog User-Defined and Enumerated Types, Arrays, structure, union, Procedural Blocks and Procedural Statements, Task and function.

UNIT- IV	System Verilog Design and Interfacing	8 hours

Modelling Finite State Machines with System Verilog, System Verilog Design Hierarchy, System Verilog Interfaces, Behavioural and Transaction Level Modelling.

UNIT-V	Verification and its Concepts	8 hours

Introduction to Verification, Types of verification, Code coverage, Introduction to task & functions in System Verilog, OOPs Terminology, Implementation of OOPs Concepts in System Verilog, Randomization, Case Studies, Assertions property, Assertions Time, Functional Coverage, FSMD methodologies and working principles, Verilog Regions, Case Studies.

Course Outcomes: After completion of this course students will be able to

CO 1	Program using C and C++ Language	K1,K2
CO 2	Simulate and Synthesize Digital Circuits	K2
CO 3	Understand System Verilog Fundamentals	K4,K6
CO 4	Design and Interfacing Digital Circuits using System Verilog	K4,K5
CO 5	Understand Verification stage and its Concepts	K1,K3

Text Books:

1. Gary K. Yeap, Practical Low Power Digital VLSI Design, KAP 2007

2. Rabaey, Pedram , "Low power design methodologies" Kluwer Academic, 1997.	
Reference Books:	
1. Kaushik Roy, Sharat Prasad, "Low-Power CMOS VLSI Circuit" Wiley 2000	
Unit 1	https://www.youtube.com/watch?v=zjyR9e-N1D4 https://www.youtube.com/watch?v=8kPo2OlvycM
Unit 2	https://www.youtube.com/watch?v=PJGvZSlsLKs https://www.youtube.com/watch?v=wiNDn19GpRU https://www.youtube.com/watch?v=dZZS8rPZQdM
Unit 3	https://www.youtube.com/watch?v=U18k9TDP5uw https://www.youtube.com/watch?v=5LUQxIDRsRI https://www.youtube.com/watch?v=a852Qb7CkTY
Unit 4	https://www.youtube.com/playlist?list=PLwdnzlV3ogoVGq4TIpX4NH6QEFYiAnyvA https://www.youtube.com/watch?v=uqNbVuuaw9w
Unit 5	https://www.youtube.com/watch?v=QwjGvzEOtKo https://www.youtube.com/watch?v=zC5b5_7oRKk https://www.youtube.com/watch?v=FWKK08X9aLk

Course Code	AMSVL0701	L T P	Credits
Course Title	VLSI Testing and Testability	3 0 0	3

Course Objective: The student will able to learn

1	Basics of testing and fault modelling
2	Testing and testability of combinational circuits
3	Testing and testability of combinational circuits
4	Built-in Self-Test (BIST), Memory and delay faults including IDDQ Testing
5	Verification using UVM

Pre-requisites: Fundamental knowledge of VLSI circuits

Course Contents/ Syllabus

UNIT-I	**Basics of Testing and Fault modelling**	**8 hours**

Introduction, Principle of testing, Types of testing, DC and AC parametric tests, Fault modelling, Stuck-at fault, Fault equivalence, Fault collapsing, Fault dominance, Fault simulation, Temporary Faults, Testing of Chips, Automatic test equipments

UNIT-II	**Testing and Testability of combinational circuits**	**8 hours**

Test generation basics, Test generation algorithms, Path sensitization, Boolean difference, D-algorithm, Testable combinational logic circuit design, The Reed Mullar Expansion Technique, Three-Level OR-AND-OR Design, Automatic Synthesis of Testing Logic, Testable Design of Multilevel Combinational Circuits, Synthesis of Random Pattern Testable Combinational Circuits, Path Delay Fault Testable Combinational Logic Design, Testable PLA Design.

UNIT-III	**Testing and Testability of Sequential Circuits**	**8 hours**

Testing of sequential circuits as iterative combinational circuits, state table verification, test generation based on circuit structure, Design of testable sequential circuits, Ad Hoc design rules, scan path technique (scan design), Partial scan, Level Sensitive Scan Design, Random Access Scan Technique, Partial Scan, Testable Sequential Circuit Design Using Non scan Techniques, Cross Check, Boundary Scan.

UNIT- IV	**Built-In Self-Test, delay fault and IDDQ testing**	**8 hours**

Test pattern generation of Built-in Self-Test (BIST), Output Response Analysis, Circular BIST, BIST Architectures.

Testable memory design, RAM fault models, test algorithms for RAMs, Delay faults, Delay test, IDDQ testing, testing methods, limitations of IDDQ Testing, BIST Techniques for Ram Chips, Test Generation and BIST for Embedded RAMs.

UNIT-V	**Verification using UVM**	**8 hours**

Introduction to Universal Verification Methodology (UVM), Transaction, Test bench & its component, UVM class factory overview, UVM reporting, Device Under Test (DUT) and its connection with environment, Scoreboards, coverage, predictors, monitors, Hierarchy in UVM, Factory Overrides, Interfaces in UVM, Configuration, Introduction of sequences, Multiple Sequences configuration, UVM register Model, RM & its use in verification, RM integration, TLM (Transaction Level Modelling).

Course Outcomes: After completion of this course students will be able to

CO 1	Understand the basics of testing and fault modelling	K1,K2
CO 2	Analyse the testing and testability of combinational circuits	K2
CO 3	Understand and analyse the testing and testability of combinational circuits	K4,K6

CO 4	Understand the Built-in Self-Test (BIST) and Memory and delay faults including IDDQ Testing	K4,K5
CO 5	Understand the Verification using UVM	K1,K3

Text Books:

1. N. K. Jha and S. G. Gupta, “Testing of Digital Systems”, Cambridge University Press.
2. M. L. Bushnell and V. D. Agrawal, “Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits”, Kluwar Academic Publishers.
3. P. K. Lala, “Digital Circuit Testing and Testability”, Academic Press.

Reference Books:

1. ZainalabeNavabi, “Digital System Test and Testable Design: Using HDL Models and Architectures”, Springer.

2.M. Abramovici, M.A. Breuer and A.D. Friedman, "Digital Systems and Testable Design", Jaico Publishing House.

Unit 1	https://www.youtube.com/watch?v=ynKZLc-wtQA, https://www.youtube.com/watch?v=lJWiYHSgVeg,
Unit 2	https://www.youtube.com/watch?v=MgCFUO2BrkQ,
Unit 3	https://www.youtube.com/watch?v=X7oB78Rq-0s, https://www.youtube.com/watch?v=molaO8iKYVQ,
Unit 4	https://www.youtube.com/watch?v=t4h1Jb5aQxM, https://www.youtube.com/watch?v=dVdnFQvHJ74,
Unit 5	https://www.youtube.com/watch?v=xAhbTylDT6k, https://www.youtube.com/watch?v=g4Pli8YgCUg,

Course Code	AMSVL0351	L T P	Credit
Course Title	Digital Integrated Circuit Lab	0 0 2	1

Course Objectives: The student will learn

1.	VLSI EDA Tool.
2.	Designing of various Logic gates.
3.	Analyze CMOS Inverter and Voltage Follower.
4.	Analysis and verification of CMOS Combinational Circuits.
5.	Analysis and verification of CMOS Sequential Circuits.

List of Experiments

Sr. No.	Name of Experiment	CO
1	Introduction to VLSI Basic and EDA Tools such as Micro Wind and or Siemens.	CO1
2	To design a 2-input NAND logic gate using 0.18 µm technology and study its DC, AC and Transient characteristics.	CO1
3	To design a 2-input NAND logic gate using 0.18 µm technology and study its DC, AC and Transient characteristics.	CO2
4	To design a 2-input NOR logic gate using 0.18 µm technology and study its Transient characteristics.	CO2
5	To design a NMOS source amplifier using 0.18 µm technology and study its DC and AC response. characteristics.	CO2
6	To design a voltage follower using 0.18 µm technology and study its DC and AC response.	CO2
7	To design a CMOS inverter using 0.18 µm technology and study its DC, AC and Transient characteristics.	CO3
8	To design and study the characteristic of CMOS XOR gate using 0.18 µm technology.	CO4
9	To design and study the characteristic of CMOS D flipflop using 0.18 µm technology.	CO3
10	To design and study the characteristic of CMOS T flipflop using 0.18 µm technology.	CO5

Course Outcome: After successful completion of this course, students will able to		**Blooms Level**
CO 1	Demonstrate VLSI EDA Tool.	K_3
CO 2	Design various Logic gates.	K_3, K_4
CO 3	Analyze CMOS Inverter and Voltage Follower.	K_3, K_4
CO 4	Analyze and verify CMOS Combinational Circuits.	K_2
CO5	Analyze and verify CMOS Sequential Circuits.	K_1, K_2, K_3

Course Code	AMSVL0451	L T P	Credit
Course Title	Advanced Digital Design Lab	0 0 2	1

Course Objectives: The student will learn

1.	Multi-vendor BOARD
2.	Interfacing of DIGITAL LOGIC with Multi-vendor Kit.
3.	interfacing of LCD (8 BIT AND 4 BIT MODE)
4.	Interfacing of RELAY & BUZZER with Multi-vendor Kit.
5.	Interfacing of GRAPHIC LCD (128x64) with Multi-vendor Kit.

List of Experiments

Sr. No.	Name of Experiment	CO
1	Introduction of Multi-vendor BOARD	CO1
2	ALTERA CYCLONE PROJECT BOARD FPGA SPARTEN 3E PROJECT BOARD FPGA SPARTEN 6S PROJECT BOARD	CO1
3	To study the interfacing of DIGITAL LOGIC with Multi-vendor Kit.	CO2
4	To study the interfacing of LCD (8 BIT AND 4 BIT MODE) with Multi-vendor Kit.	CO2
5	To study the interfacing of LCD + (4X4) KEYPAD with Multi-vendor Kit.	CO2
6	To study the interfacing of RELAY & BUZZER with Multi-vendor Kit.	CO2
7	To study the interfacing of 7-SEGMENT+KEYBOARD with Multi-vendor Kit.	CO3
8	To study the interfacing of DAC 0808 with Multi-vendor Kit.	CO4
9	To study the interfacing of GRAPHIC LCD (128x64) with Multi-vendor Kit.	CO3
10	To study the interfacing of VGA with Multi-vendor Kit.	CO5

Course Outcome: After successful completion of this course, students will able to		**Blooms Level**
CO 1	Demonstrate Multi-vendor BOARD.	K_3
CO 2	Interface DIGITAL LOGIC with Multi-vendor Kit.	K_3, K_4
CO 3	Interface LCD (8 BIT AND 4 BIT MODE)	K_3, K_4
CO 4	Interface RELAY & BUZZER with Multi-vendor Kit.	K_2
CO5	Interface GRAPHIC LCD (128x64) with Multi-vendor Kit.	K_1, K_2, K_3

Course Code	AMSVL0551	L T P	Credit
Course Title	Digital Design using VHDL/Verilog Lab	0 0 2	1

Course Objectives: The student will learn

1.	About basics of VHDL/Verilog.
2.	To design basic digital logic gates and adder circuits using VHDL/Verilog.
3.	To design various combinational circuits using VHDL/Verilog.
4.	To design various sequential circuits using VHDL/Verilog.
5.	To design memory module.

List of Experiments

Sr. No.	Name of Experiment	CO
1	To simulate and synthesis the HDL description of basic logic gates using VHDL/Verilog through behavioral modeling.	CO1
2	To simulate and synthesis the HDL description of half adder and full adder using VHDL/ Verilog through structural modeling.	CO1
3	To simulate and synthesis the HDL description of 4:1 Multiplexer and 1:4 demultiplexer using VHDL/ Verilog.	CO2
4	To simulate and synthesis the HDL description of 16:1 Multiplexer and 1:16 demultiplexer using VHDL/ Verilog.	CO2
5	To simulate and synthesis the HDL description of 3-bit ripple carry adder using VHDL/Verilog through port mapping.	CO2
6	To simulate and synthesis the HDL description of SR latch with NOR gates with port mapping using VHDL/Verilog.	CO2
7	To simulate and synthesis the HDL description of positive edge triggered JK flip-flop using case statement.	CO3
8	To simulate and synthesis the HDL description of 3-bit synchronous counter using VHDL/Verilog.	CO4
9	To simulate and synthesis the HDL description of decade counter: a) Synchronous b) Asynchronous.	CO3
10	To simulate and synthesis the HDL description of N-bit memory word using generate.	CO5

Course Outcome: After successful completion of this course, students will able to		**Blooms Level**
CO 1	Know the basics of VHDL/Verilog.	K_3
CO 2	Design basic digital logic gates and adder circuits using VHDL/Verilog.	K_3, K_4
CO 3	Design various combinational circuits using VHDL/Verilog.	K_3, K_4
CO 4	Design various sequential circuits using VHDL/Verilog.	K_2
CO5	Design memory module.	K_1, K_2, K_3