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NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA (An Autonomous Institute Affiliated to AKTU, Lucknow) B.Tech. SEM: III - THEORY EXAMINATION (2021 - 2022) (ONLINE) Subject: Digital System Design Time: 02:00 Hours Max. Marks: 100 General Instructions: 1. All questions are compulsory. It comprises of two Sections A and B. • Section A - Question No- 1 has 35 objective type questions carrying 2 marks each. • Section B - Question No- 2 has 12 subjective type questions carrying 3 marks each. You have to attempt any 10 out of 12 question. • No sheet should be left blank. Any written material after a Blank sheet will not be evaluated/checked. $35 \ge 2 = 70$ SECTION A 1. Attempt ALL parts:-Hamming code is capable of (CO1) 1.1.a 1 (a) Only detect single-bit error (b) Only correct single-bit error (c) Detect and correct single bit error (d) Detect and correct multiple bit errors 1 1.1.b The logical expression $Y = \sum m(0, 3, 6, 7, 10, 12, 15)$ is equivalent to (a) $\pi M(0, 3, 6, 7, 10, 12, 15)$ (b) π **M**(1, 2, 4, 5, 8, 9, 11, 13, 14) (c) $\Sigma m(1, 2, 4, 5, 8, 9, 11, 13, 14)$ (d) $\Sigma m(0, 2, 4, 6, 8, 10, 12, 14)$ 1.1.c Find the 2's complement of 1101011101000. (CO1) 1 (a) 1101011101000 (b) 1001011101000 (c) 1011101001 (d) None of these Find the binary equivalent of decimal number 0.875 1.1.d 1 (a) 0.111 (b) 0.0101 (c) 01.0101 (d) 1.0101 The SOP form of logical expression is most suitable for designing logic circuits using only 1.1.e 1 (a) XOR gates (b) AND gates (c) NAND gates (d) NOR gates 1.1.f How many AND gates are required to realize Y = CD + EF + G? 1 (a) 4

(b) 5

(c) 3 (d) 2 1.1.g A switching function f(A, B, C, D) = A'B'CD + A'BC'D + AB'C'D + AB'CD + A'BCD can1 also be written as (a) $\Sigma m(1, 3, 5, 7, 9)$ (b) $\Sigma m(3, 5, 7, 9, 11)$ (c) $\Sigma m(3, 5, 9, 11, 13)$ (d) None of these 1.2.a How many data select lines are required for selecting eight inputs? 1 (a) 1 (b) 2(c) 3 (d) 4 1.2.b A half adder circuit has two inputs and 1 (a) one output (b) two output (c) three output (d) none of these 1.2.c In four-variable K-map simplification, a group of eight adjacent ones leads to a term 1 with (CO2) (a) one literal (b) two literal (c) three literal (d) four literal 1.2.d For a 4-bit parallel adder, if the carry-in is connected to a logical HIGH, the result is: 1 (a) The same as if the carry-in is tied LOW since the least significant carry-in is ignored. (b) That carry-out will always be HIGH (c) One will be added to the final result. (d) The carry-out is ignored. 1.2.e The binary subtraction 0 - 1 =1 (a) difference = 0, borrow = 0(b) difference = 1, borrow = 0(c) difference = 1, borrow = 1(d) difference = 0, borrow = 11.2.f How many NAND gates are needed to implement a full adder? 1 (a) 12 (b) 13 (c) 14 (d) 15 1

A code converter is a logic circuit that _____ 1.2.g

- (a) Inverts the given input
- (b) Converts into decimal number
- (c) Converts data of one type into another type
- (d) Converts to octal
- 1.3.a Why latches are called memory devices?
 - (a) It has capability to stare 8 bits of data

1

| | (b) It has internal memory of 4 bit(c) It can store one bit of data | |
|-------|---|---|
| | (d) It can store infinite amount of data | |
| 1.3.b | When both inputs of SR latches are high, the latch goes (CO3) | 1 |
| | (a) Unstable | |
| | (b) Stable | |
| | (c) Indeterminate state | |
| | (d) Bistable | |
| 1.3.c | How many types of sequential circuits are? | 1 |
| | (a) 2 | |
| | (b) 3 | |
| | (c) 4 | |
| | (d) 5 | |
| 1.3.d | What is a trigger pulse? (CO3) | 1 |
| | (a) A pulse that starts a cycle of operation | |
| | (b) A pulse that reverses the cycle of operation | |
| | (c) A pulse that prevents a cycle of operation | |
| | (d) A pulse that enhances a cycle of operation | |
| 1.3.e | The difference between a flip-flop & latch is | 1 |
| | (a) Both are same | |
| | (b) Flip-flop consist of an extra output | |
| | (c) Latches has one input but flip-flop has two | |
| | (d) Latch has two inputs but flip-flop has one | |
| 1.3.f | What is one disadvantage of an S-R flip-flop? | 1 |
| | (a) It has no Enable input | |
| | (b) It has a RACE condition | |
| | (c) It has no clock input | |
| 1.0 | (d) Invalid State | 1 |
| 1.3.g | What is the hold condition of a flip-flop? | 1 |
| | (a) Both S and R inputs activated | |
| | (b) No active S or R input | |
| | (c) Only S is active | |
| 140 | (d) Only K is active The basic function of TTL gate is which of the following functions? $(CO4)$ | 1 |
| 1.4.a | (c) AND | 1 |
| | (a) AND (b) OP | |
| | (b) OK (c) NOR | |
| | (d) NAND | |
| 14b | Which of the following is the propagation delay of TTL circuits? | 1 |
| 1.4.0 | (a) 1 s | 1 |
| 1.4.c | (a) 1 s (b) 1 ms | |
| | (c) 1 ns | |
| | (d) 1 ps | |
| | The logic '0' of ECL is represented as V and logic '1' is represented as V | 1 |
| | (a) 1, 1.65 | 1 |
| | (b) 0.9, 1.75 | |
| | | |

| | (c) 1.2, 2.35 (l) 1.0, 4.2 | |
|-------|--|---------|
| 111 | $(\mathbf{d}) 1.9, 4.3$ | 1 |
| 1.4.0 | | 1 |
| | (a) NOT gate (b) OP gate | |
| | (b) OK gate | |
| | (d) None of the above | |
| 1.4.e | Which of the following logic families has the highest fan-out? | 1 |
| | (a) TTL | |
| | (b) CMOS | |
| | (c) ECL | |
| | (d) Schottky TTL | |
| 1.4.f | Which of the following statements is incorrect? | 1 |
| | (a) TTL logic has very low power consumption and is therefore widely used in integrated components | highly |
| | (b) TTL devices have logic levels of about 3.4 V and 0.2V | |
| | (c) TTL logic normally operates from a single 5V supply. | |
| | (d) standard TTL devices have a propagation delay that is dominated by the storage the bipolar transistors used. | time of |
| 1.4.g | Which of the following logic family dissipates minimum power? | 1 |
| | (a) CMOS | |
| | (b) ECL | |
| | (c) TTL | |
| | (d) DTL | |
| 1.5.a | A Flip flop stores number of bits. | 1 |
| | (a) one | |
| | (b) two | |
| | (c) three | |
| 1 - 1 | (d) Iour | |
| 1.5.b | How many 1024 * 1 RAM chips are required to construct a 1024 * 8 memory system? | 1 |
| | (a) 4 | |
| | (b) 8 | |
| | (c) 10 (d) 0 | |
| 150 | (u) \mathcal{F} | 1 |
| 1.5.0 | (c) 10 | 1 |
| | (a) 10 (b) 13 | |
| | (0) 13 | |
| | $\begin{pmatrix} \mathbf{d} \\ \mathbf{q} \end{pmatrix} \mathbf{q}$ | |
| 15d | Elash memory is Also Known as | 1 |
| 1.3.u | (a) Elech DAM | 1 |
| | (a) Flash RAM | |
| | (c) Flash DROM | |
| | (d) Flash SRAM | |
| 15e | Memory is a part of | 1 |
| 1.5.0 | (a) Input device | 1 |
| | (a) input device | |

| | (b) Output device | |
|---------|--|---|
| | (c) CPU | |
| | (d) Control Unit | |
| 1.5.f | Which of the following medium is used between CPU & RAM to speed up the processing power of a CPU ? | 1 |
| | (a) Virtual Memory | |
| | (b) DRAM | |
| | (c) Flash Memory | |
| | (d) Cache Memory | |
| 1.5.g | What is the permanent memory built into your computer called ? | 1 |
| | (a) RAM | |
| | (b) ROM | |
| | (c) CPU | |
| | (d) CD-ROM | |
| | $\underline{\text{SECTION B}} \qquad \qquad 10 \text{ X 3} = 30$ | |
| 2. Answ | er any <u>TEN</u> of the following:- | |
| 2.1.a | Write the truth table of BCD (2421) code? | 2 |
| 2.1.b | Draw the logical circuit of OR Gate using NAND Gate | 2 |
| 2.2.a | List out the different combinational logic circuits. | 2 |
| 2.2.b | $F(X,Y,Z)=\prod M(0,1,2,4)$ minimize the given using K-MAP in POS form. | 2 |
| 2.2.c | What is the major difference between half-adders and full-adders? | 2 |
| 2.3.a | What is Excitation Table of Flip Flops? | 2 |
| 2.3.b | Design a MOD-10 ripple counter. | 2 |
| 2.3.c | what is Synchronous counter ? | 2 |
| 2.4.a | Compare TTL and CMOS logic families on the basis of following: i) Propogation delay ii) Power dissipation iii) Fan-out iv) Basic gate | 2 |
| 2.4.b | Write the advantages of Totem pole arrangment. | 2 |
| 2.5.a | Mention the two types of erasable PROM. | 2 |
| 2.5.b | Classify PLDs. | 2 |
| | | |