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NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech.

SEM: III - THEORY EXAMINATION (2021 - 2022) (ONLINE)

Subject: Computer Organization & Architecture

Time: 02:00 Hours

Max. Marks: 100

General Instructions:

1. All questions are compulsory. It comprises of two Sections A and B.
 - Section A - Question No- 1 has 35 objective type questions carrying 2 marks each.
 - Section B - Question No- 2 has 12 subjective type questions carrying 3 marks each. You have to attempt any 10 out of 12 question.
 - No sheet should be left blank. Any written material after a Blank sheet will not be evaluated/checked.

SECTION A

35 x 2 = 70

1. Attempt ALL parts:-

- | | | |
|-------|--|---|
| 1.1.a | Brain of computer is (CO1) | 1 |
| | (a) Control unit | |
| | (b) Arithmetic and Logic unit | |
| | (c) Central Processing Unit | |
| | (d) Memory | |
| 1.1.b | The functions of execution and sequencing are performed by using _____ | 1 |
| | (a) Input Signals | |
| | (b) Output Signals | |
| | (c) Control Signals | |
| | (d) CPU | |
| 1.1.c | Which unit is responsible for converting the data received from the user into a computer understandable format?(CO1) | 1 |
| | (a) Memory Unit | |
| | (b) Arithmetic & Logic Unit | |
| | (c) Output Unit | |
| | (d) Input Unit | |
| 1.1.d | The third state of a Three-state Buffer is _____ | 1 |
| | (a) 0 | |
| | (b) High Impedance | |
| | (c) 1 | |
| | (d) Short circuit | |
| 1.1.e | Saving data and instructions to make them readily available is the job of _____ | 1 |
| | (a) Cache Unit | |
| | (b) Storage Unit | |
| | (c) Input Unit | |
| | (d) Output Unit | |
| 1.1.f | The addressing mode in which the operands are in registers that reside within the CPU. | 1 |
| | (a) Register addressing mode | |
| | (b) Index addressing mode | |

	(c) Relative addressing mode	
	(d) Implied addressing mode	
1.1.g	The addressing mode in which the operands are specified implicitly in the instruction.	1
	(a) Indirect addressing mode	
	(b) Index addressing mode	
	(c) Relative addressing mode	
	(d) Implied addressing mode	
1.2.a	The 'heart' of the processor which performs many different operations	1
	(a) Arithmetic and logic unit	
	(b) Motherboard	
	(c) Control Unit	
	(d) Memory	
1.2.b	When we perform subtraction on -7 and -5 the answer in 2's complement form is	1
	(a) 11110	
	(b) 1110	
	(c) 1010	
	(d) 1000	
1.2.c	The sign magnitude representation of -9 is	1
	(a) 10000	
	(b) 10010	
	(c) 10111	
	(d) 11011	
1.2.d	 is used for binary multiplication?	1
	(a) Restoring Multiplication	
	(b) Booth's Algorithm	
	(c) Pascal's Rule	
	(d) Digit-by-digit multiplication	
1.2.e	Carry lookahead adder uses the concepts of (CO2)	1
	(a) Inverting the inputs	
	(b) Complementing the outputs	
	(c) Generating and propagating carries	
	(d) None of the mentioned	
1.2.f	IEEE stands for _____	1
	(a) Instantaneous Election Electrical Engineering	
	(b) Institute of Emerging Electrical Engineers	
	(c) Institute of Emerging Electronic Engineers	
	(d) Institute of Electrical and electronics engineers	
1.2.g	IEEE 754 representation for _____	1
	(a) Floating Point No.	
	(b) Integer no.	
	(c) Binary no.	
	(d) Octal no.	
1.3.a	Two important fields of an instruction are (CO3)	1
	(a) Opcode	
	(b) Operand	
	(c) mode	

	(d) Both 1 & 2	
1.3.b	Group of binary bits(0&1) is known as (a) Binary code (b) Digit code (c) Symbolic representation (d) None of these	1
1.3.c	Pipe-lining is a unique feature of _____ (a) CISC (b) RISC (c) ISA (d) ANNA	1
1.3.d	In micro-programmed approach, the signals are generated by (a) Machine instructions (b) System programs (c) Utility tools (d) None of the mentioned	1
1.3.e	Highly encoded schemes that use compact codes to specify a small number of functions in each micro instruction is (a) Horizontal organisation (b) Vertical organisation (c) Diagonal organisation (d) None of the mentioned	1
1.3.f	___ register holds the Next instruction to be executed (a) TR (b) AR (c) PC (d) None	1
1.3.g	The processing speed of a computer depends on the _____of the system (a) Clock speed (b) Speed (c) Booting (d) None	1
1.4.a	What is true about memory unit (a) A memory unit is the collection of storage units or devices together (b) The memory unit stores the binary information in the form of bits. (c) 1& 2 (d) None of the above	1
1.4.b	When power is switched off which memory loses its data (a) Non-Volatile Memory (b) Volatile Memory (c) Both A and B (d) None of the above	1
1.4.c	What is the formula for Hit Ratio? (CO4) (a) Hit/(Hit + Miss) (b) Miss/(Hit + Miss) (c) (Hit + Miss)/Miss	1

- (d) (Hit + Miss)/Hit
- 1.4.d Which of the following is correct example for Auxiliary Memory 1
- (a) Magnetic disks
 - (b) Tapes
 - (c) Flash memory
 - (d) Both 1 and 2
- 1.4.e 2k* 8 ROM chips which are required to built a 16K*8 memory system are of number 1
- (a) 2
 - (b) 4
 - (c) 8
 - (d) 16
- 1.4.f Address bits needed to select all memory locations in 16K * 1 RAM are (CO4) 1
- (a) 8
 - (b) 10
 - (c) 14
 - (d) 16
- 1.4.g The secondary memory of a computer can act as a 1
- (a) Cache
 - (b) virtual memory
 - (c) RAM
 - (d) ROM
- 1.5.a In memory-mapped I/O (CO5) 1
- (a) The I/O devices have a separate address space
 - (b) A part of the memory is specifically set aside for the I/O operation
 - (c) The I/O devices and the memory share the same address space
 - (d) The memory and I/O devices have an associated address space
- 1.5.b The _____ input is used by the DMA controller to request the CPU to relinquish control of the buses. 1
- (a) Bus Grant
 - (b) Bus request
 - (c) Burst Transfer
 - (d) Data Input
- 1.5.c A _____ command is issued to activate the peripheral and to inform it what to do. 1
- (a) Control
 - (b) Status
 - (c) Data output
 - (d) Data Input
- 1.5.d A hand-shake based protocol for data transfer is an example of _____ type of data transfer. 1
- (a) Parallel
 - (b) Synchronous
 - (c) Asynchronous
 - (d) Serial
- 1.5.e In _____ data transmission, each bit of the message has its own path and the total message is transmitted at the same time. 1
- (a) Parallel
 - (b) Serial

- (c) Asynchronous
(d) None
- 1.5.f In Daisy Chaining Priority, the device with the highest priority is placed at the _____. 1
 (a) Last Position
 (b) Can be placed anywhere
 (c) First Position
 (d) Depend on device
- 1.5.g In _____ transmission, the two units share a common clock frequency and bits are 1
 transmitted continuously at the rate dictated by the clock pulses.
 (a) Parallel
 (b) Serial
 (c) Synchronous
 (d) Asynchronous

SECTION B

10 X 3 = 30

2. Answer any TEN of the following:-

- 2.1.a A digital computer has a common bus system for 16 registers of 32 bits each. The bus is 2
 constructed with multiplexers.
 a. How many multiplexers are there in the bus?
 b. What size of multiplexers are needed?
- 2.1.b Write the sequence of microoperation for implementation of POP operation in register stack. 2
- 2.2.a What is the value of 11010010 after circular shift left and right? 2
- 2.2.b Explain the hardware diagram of signed magnitude multiplication algorithm 2
- 2.2.c Explain the Advantages and Disadvantages of CLA. 2
- 2.3.a What are the differences between the hardwired control organization and micro programmed 2
 Control organization.
- 2.3.b Define Memory address register.(CO3) 2
- 2.3.c Draw the flow of Instruction cycle. 2
- 2.4.a Define tag in cache mapping.(CO4) 2
- 2.4.b Define role of key register in associative memory. 2
- 2.5.a Explain the term cycle stealing and burst transfer. (CO5) 2
- 2.5.b Why are the read and write control lines in DMA bidirectional? 2