Printed Page:- Subject Code:- ACSE0304

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech.

SEM: III - THEORY EXAMINATION (2021 - 2022) (ONLINE)

Subject: Digital Logic & Circuit Design

Time: 02:00 Hours Max. Marks: 100

General Instructions:

1. *All questions are compulsory. It comprises of two Sections A and B.*

- *Section A - Question No- 1 has 35 objective type questions carrying 2 marks each.*
- *Section B - Question No- 2 has 12 subjective type questions carrying 3 marks each. You have to attempt any 10 out of 12 question.*
- *No sheet should be left blank. Any written material after a Blank sheet will not be evaluated/checked.*

SECTION A 35 x 2 = 70

1. Attempt ALL parts:-

1.1.a Hamming code is capable of 1

(a) Only detect single-bit error
(b) Only correct single-bit error
(c) Detect and correct single bit error
(d) **Detect and correct multiple bit errors**

1.1.b Find the 2's complement of 1101011101000 1

(a) 1101011101000
(b) 1001011101000
(c) 1011101001
(d) None of these

1.1.c Find the binary equivalent of decimal number 0.3125 1

(a) 0.1101
(b) 0.0101
(c) 1.0101
(d) 1.0111

1.1.d The ASCII code is basically a 1

(a) 7-bit code
(b) 12-bit code
(c) 4-bit code
(d) 6-bit code

1.1.e In four-variable K-map simplification, a group of eight adjacent ones leads to a term with 1

(a) one literal less than the total number of variables
(b) two literals less than the total number of variables
(c) three literals less than the total number of variables
(d) four literals less than the total number of variables

1.1.f Complement of the expression A'B + CD' is _____ 1

(a) (A + B')(C' + D)
(b) (A + B)(A + C)
(c) 0

(d) 0,0

1.1.g Using the transformation method you can realize any POS realization of OR-AND with only 1

(a) Digital
(b) Diagonal
(c) Venn Diagram
(d) NOR

1.2.a How many data select lines are required for selecting eight inputs? (CO2) 1

(a) 1
(b) 2
(c) 3
(d) 4

1.2.b A half adder circuit has two inputs and 1

(a) one output
(b) two output
(c) three output
(d) none of these

1.2.c 7483 IC ? 1

(a) 4 Bit binary full adder
(b) NAND
(c) 2 Bit binary half adder
(d) DEMUX

1.2.d The output of SUM is equal to output of 1

(a) OR gate
(b) AND gate
(c) X-OR gate
(d) X-Nor gate

1.2.e For a 4-bit parallel adder, if the carry-in is connected to a logical HIGH, the result is: 1

(a) The same as if the carry-in is tied LOW since the least significant carry-in is ignored.
(b) That carry-out will always be HIGH
(c) One will be added to the final result.
(d) The carry-out is ignored.

1.2.f The binary subtraction 0 – 1 = 1

(a) difference = 0, borrow = 0
(b) difference = 1, borrow = 0
(c) difference = 1, borrow =1
(d) difference = 0, borrow = 1

1.2.g Which combinational circuit is renowned for selecting a single input from multiple inputs & directing the binary information to single output line? 1

(a) Multiplexer
(b) Data distributor
(c) Both data selector and data distributor
(d) DeMultiplexer

1.3.a Which circuit is generated from D flip-flop due to addition of an inverter by causing reduction in the number of inputs? 1

(a) Gated JK-latch
(b) Gated SR-latch

(c) Gated T-latch
(d) Gated D-latch

1.3.b When is a flip-flop said to be transparent? (CO3) 1

(a) When the Q output is opposite the input
(b) When the Q output follows the input
(c) When you can see through the IC packaging
(d) When the Q output is complementary of the input

1.3.c What is one disadvantage of an S-R flip-flop? 1

(a) It has no Enable input
(b) It has a RACE condition
(c) It has no clock input
(d) Invalid State

1.3.d A universal register 1

(a) accepts serial input
(b) accepts parallel input
(c) gives serial and parallel outputs
(d) is capable of all of the above

1.3.e A ring counter consisting of five flip-flops will have 1

(a) 10 states
(b) 5 states
(c) 25 states
(d) none of the above

1.3.f How many types of sequential circuits are? 1

(a) 2
(b) 3
(c) 4
(d) 5

1.3.g When both inputs of SR latches are high, the latch goes _____ 1

(a) Unstable
(b) Stable
(c) Metastable
(d) Bistable

1.4.a If some or all the outputs of a sequential circuit do not change affect with respect to active transition of clock signal, then that sequential circuit is called as 1

(a) Asynchronous sequential circuit
(b) Synchronous sequential circuit
(c) Any of these
(d) None of these

1.4.b In a down counter, which flip-flop doesn't toggle when the inverted output of the preceeding flip-flop goes from HIGH to LOW. 1

(a) MSB flip-flop
(b) LSB flip-flop
(c) Master slave flip-flop
(d) Latch

1.4.c In a T flip-flop the output frequency is 1

(a) same as the input frequency

(b) one-half its inputs frequency
(c) double the input frequency
(d) none of the above

1.4.d How many types of resets are there in hardware design? 1

(a) One
(b) Two
(c) Three
(d) Four

1.4.e In synchronous reset, reset is sampled with respect to _____ 1

(a) Enable signal
(b) Data input signal
(c) Clock signal
(d) Output signal

1.4.f Which of the following is an advantage of a synchronous reset? 1

(a) It is slow
(b) It requires a clock signal to reset the circuit
(c) It filters the reset signal
(d) It needs a stretched reset

1.4.g In which model, the next state is a function of the present state and the present inputs. Its output is also a function of the present state and the present inputs. 1

(a) Mealy Circuit model
(b) Moore Circuit Model
(c) Both of these
(d) None of these

1.5.a Which of the following has the lowest access time? 1

(a) RAM
(b) ROM
(c) Registers
(d) Flag

1.5.b Main memories of a computer, usually made up of _____ 1

(a) Registers
(b) Semiconductors
(c) Counters
(d) PLDs

1.5.c As the storage capacity of the main memory is inadequate, which memory is used to enhance it? 1

(a) Secondary Memory
(b) Auxiliary Memory
(c) Static Memory
(d) Both Secondary Memory and Auxiliary Memory

1.5.d Which memories are if magnetic memory type? 1

(a) Main Memory
(b) Secondary Memory
(c) Static Memory
(d) Volatile Memory

1.5.e Which of the following comes under secondary memory/ies? (CO5) 1

(a) Floppy disk
(b) Magnetic drum
(c) Hard disk
(d) All of the Mentioned

1.5.f A sequential access memory is one in which _____ 1

(a) A particular memory location is accessed rapidly
(b) A particular memory location is accessed sequentially
(c) A particular memory location is accessed serially
(d) A particular memory location is accessed parallely

1.5.g Which of the following memories is non-volatile memory? 1

(a) ROM
(b) PROM
(c) ferrite core memory
(d) none of the above

SECTION B 10 X 3 = 30

2. Answer any TEN of the following:-

2.1.a	Perform the octal subtraction of 6753-4675	2
2.1.b	Draw the logical circuit of X-OR Gate using NAND Gate	2
2.2.a	Design 8 x 1 MUX using 4 x 1 MUX.	2
2.2.b	Design 2 bit binary comparator.	2
2.2.c	Design a MOD-5 ripple counter.	2
2.3.a	Explain Race Around Condition in J-K flip-flop.	2
2.3.b	Design MOD-5 synchronous counter using T flip flop.	2
2.3.c	Derive the characteristic equation of SR flip-flop.	2
2.4.a	Why hazards occur in a circuit?	2
2.4.b	Compare synchronous and asynchronous sequential circuits.	2
2.5.a	Write short notes on PLDs.	2
2.5.b	How many 16K * 4 RAMs are required to achieve a memory with a capacity of 64K and a word length of 8 bits? (CO5)	2