Printed Page:- Subject Code:- ACSBS0303

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech.

SEM: III - THEORY EXAMINATION (2021 - 2022) (ONLINE)

Subject: Computer Organization & Architecture

Time: 02:00 Hours Max. Marks: 100

General Instructions:

1. *All questions are compulsory. It comprises of two Sections A and B.*

- *Section A - Question No- 1 has 35 objective type questions carrying 2 marks each.*
- *Section B - Question No- 2 has 12 subjective type questions carrying 3 marks each. You have to attempt any 10 out of 12 question.*
- *No sheet should be left blank. Any written material after a Blank sheet will not be evaluated/checked.*

SECTION A 35 x 2 = 70

1. Attempt ALL parts:-

1.1.a The functions of execution and sequencing are performed by using _____ 1

(a) Input Signals
(b) Output Signals
(c) Control Signals
(d) CPU

1.1.b Which unit is responsible for converting the data received from the user into a computer understandable format? 1

(a) Memory Unit
(b) Arithmetic & Logic Unit
(c) Input Unit
(d) Output Unit

1.1.c One nibble is equivalent to how many bits? 1

(a) 2
(b) 4
(c) 8
(d) 1

1.1.d The output unit converts the data entered by the user into computer understandable form. 1

(a) True
(b) FALSE

1.1.e _____ BUS arbitration approach uses the involvement of the processor. 1

(a) Centralised arbitration
(b) Distributed arbitration
(c) Random arbitration
(d) All of the mentioned

1.1.f Which of the following is non-volatile storage? 1

(a) Backup
(b) Secondary
(c) Primary
(d) Cache

1.1.g	What does the symbol D represent in a hexadecimal number system? (CO1) (a) 8 (b) 16 (c) 13 (d) 14	1
1.2.a	Booth's Algorithm is applied on decimal numbers. (a) TRUE (b) FALSE	1
1.2.b	The 1's complement of 1 in 4 bits is 1110. (a) TRUE (b) FALSE	1
1.2.c	The value of n in multiplication of 110* 1000 is 4. (a) TRUE (b) FALSE	1
1.2.d	The summing outputs of a half or full-adder are designated by which Greek symbol Theta (a) TRUE (b) FALSE	1
1.2.e	When 1101 is used to divide 100010010 the remainder is 1. (a) TRUE (b) FALSE	1
1.2.f	IEEE stands for _____ (a) Instantaneous Election Electrical Engineering (b) Institute of Emerging Electrical Engineers (c) Institute of Emerging Electronic Engineers (d) Institute of Electrical and electronics engineers	1
1.2.g	In both signed magnitude and 2's complement , positive and negative numbers are separated using _____ (a) LSB (b) MSB (c) 0 (d) 1	1
1.3.a	In a 4M-bit chip organisation has a total of 19 external connections.then it has 9 address if 8 data lines are there. (a) TRUE (b) FALSE	1
1.3.b	If going fully associative, refers to the fully associative (a) TRUE (b) FALSE	1
1.3.c	The software that supports virtual machines is called kernel. (a) TRUE (b) FALSE	1
1.3.d	In computer, CCD stands for charge couple device (a) TRUE (b) FALSE	1
1.3.e	The instruction miss which is serviced by the main memory has total latency, approximately of ____ processor cycle	1

(a) 10
(b) 35
(c) 1
(d) 0

1.3.f CPU performance is often measured in _____ & _____ 1

(a) MIPS and BIPS
(b) LISP
(c) LIFO
(d) None

1.3.g Address bits needed to select all memory locations in the 2118 16K * 1RAM are 1

(a) 8
(b) 10
(c) 14
(d) 16

1.4.a The main job of the interrupt system is to identify the _____ of the interrupt. 1

(a) Source
(b) Signal
(c) Device
(d) Peripherals

1.4.b In Daisy Chaining Priority, the device with the highest priority is placed at the _____. 1

(a) Last Position
(b) Can be placed anywhere
(c) First Position
(d) Depend on device

1.4.c A hand-shake based protocol for data transfer is an example of _____ type of data transfer. (CO4) 1

(a) Parallel
(b) Synchronous
(c) Asynchronous
(d) Serial

1.4.d When the R/W bit of the status register of the DMA controller is set to 1. 1

(a) Device interface
(b) Data controller
(c) DMA controller
(d) Overlooker

1.4.e How many types of modes of I/O Data Transfer 1

(a) 3
(b) 2
(c) 5
(d) 4

1.4.f Input or output devices attached to the computer are also called _____ 1

(a) Interrupt
(b) Secondary storage devices
(c) Peripheral Devices
(d) Memory

1.4.g The processor indicates to the devices that it is ready to receive interrupts by activating the interrupt acknowledge line 1

(a) TRUE

(b) FALSE

1.5.a In a vertical microinstruction, a code is used for each action to be performed and the decoder translates this code into individual control signals. 1

(a) TRUE

(b) FALSE

1.5.b In a horizontal microinstruction every bit in the control field attaches to a control line 1

(a) TRUE

(b) FALSE

1.5.c Microprogrammed control unit and Hardwired control unit are logically similar and have the same execution speed. (CO5) 1

(a) TRUE

(b) FALSE

1.5.d To increase the speed of memory access in pipelining, we make use of Cache 1

(a) TRUE

(b) FALSE

1.5.e In pipelining the task which requires the least time is performed first. 1

(a) TRUE

(b) FALSE

1.5.f Each stage in pipelining should be completed within one cycle. 1

(a) TRUE

(b) FALSE

1.5.g The name hardwired came because the sequence of operations carried out is determined by the wiring. 1

(a) TRUE

(b) FALSE

SECTION B 10 X 3 = 30

2. Answer any TEN of the following:-

2.1.a What is Virtual Memory In Computer? 2

2.1.b Define positive logic and negative logic. 2

2.2.a Define multiplication algorithm which including sign bit in all process. 2

2.2.b Draw 2 bit by 2 bit array multiplier. 2

2.2.c Explain block diagram of Half Adder. 2

2.3.a Explain the role of ROM in the system start up process. 2

2.3.b Explain the concept of direct mapping of cache memory. (CO3) 2

2.3.c Explain the set associative cache mapping using block diagram and example. 2

2.4.a Explain DMA transfer in a computer system with help of a diagram. 2

2.4.b Explain CPU - IOP Communication. Draw the flowchart showing the sequence of operations to be carried out. 2

2.5.a Explain SISD in computer system 2

2.5.b Define speed up and efficiency. 2