Printed page: 02 **Subject Code: AMTVL0112**

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NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

MASTER OF TECHNOLOGY (M.Tech)

(SEM: FIRST; Theory Examination (2020-2021)

SUBJECT NAME: MOS DEVICE MODELLING

Time: 3Hours **Max. Marks: 70**

General Instructions:

- All questions are compulsory. Answers should be brief and to the point.
- This Question paper consists of ...02...pages & ...08.....questions.
- It comprises of three Sections, A, B, and C. You are to attempt all the sections.
- Section A -Question No- 1 is objective type questions carrying 1 mark each, Question No- 2 is very short answer type carrying 2 mark each. You are expected to answer them as directed.
- Section B - Question No-3 is Long answer type -I question with external choice carrying 4marks each. You need to attempt any five out of seven questions given.
- Section C -Question No. 4-8 are Long answer type –II (within unit choice) questions carrying 7marks each. You need to attempt any one part *a* or *b*.
- Students are instructed to cross the blank sheets before handing over the answer sheet to the invigilator.
- No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION -A

1. Attempt all parts- **[5x1=5]** **CO**

a. In ratioed logic the entire pull-up-network is replaced by? **(1)** **CO2**
(1) single unconditional load
(2) Nothing
(3) Pull down network
(4) All of the above

b. What are the techniques to reduce the switching activity factor? **(1)** **CO1**
(1) Logic restructuring
(2) Input ordering
(3) Time multiplexing
(4) All of the above

c. Statement: Sizing is only effective when the load is dominated by the fan-out. Is the given statement true or false? **(1)** **CO2**
(1) True
(2) False

d. Which type of MOSFET structure is best for high performance application? **(1)** **CO4**
(1) PD SOI
(2) FD SOI
(3) FinFet
(4) NCFET

e. How lambda λ can be represented in VLSI design? **(1)** **CO4**

2. Attempt all parts- **[5x2=10]**

a.	What is the need of Layouts?	**(2)**	**CO1**
b.	What is photolithography?	**(2)**	**CO2**
c.	Which is better from NAND and NOR logic gates? Justify your answer.	**(2)**	**CO2**
d.	Define constant voltage scaling of MOS device.	**(2)**	**CO3**
e.	Why selection of W/L ratio of a MOS device is critical?	**(2)**	**CO5**

SECTION -B

3. Answer any five of the following-		**[5x4=20]**	**CO**
a.	Explain the I-V characteristics of FinFET device and compare it with n-channel enhancement type MOSFET. Also, derive the mathematical relationship for the drain current.	**(4)**	**CO4**
b.	How velocity saturated MOS models are different from normal long channel MOS models?	**(4)**	**CO3**
c.	Consider an n channel MOSFET with following characteristics: t_{ox}=10 nm, μ_n=520 cm^2 /V-s, (W/L)=8,V_{Th}=+0.70V,V_{gsn}=2V and V_{dsn}=2V. Find the drain source current.	**(4)**	**CO5**
d.	What is pass transistor logic? Why it is preferred over NMOS/PMOS switch?	**(4)**	**CO2**
e.	Explain, how VTC of CMOS inverter is impacted the device aspect ratio?	**(4)**	**CO4**
f.	Explain about non ideal effects in a MOS device.	**(4)**	**CO3**
g.	Define the latch up problem in CMOS and explain how it can be avoided.	**(4)**	**CO2**

SECTION-C

4. Answer any one of the following-		**[5x7=35]**	
a.	Describe twin tub process for fabrication of the CMOS transistor with suitable diagram.	**(7)**	**CO2**
b.	Explain the second order effects in MOSFETs.	**(7)**	**CO5**
5. Answer any one of the following-			
a.	Define and derive the switching inverter delay for a CMOS configuration.	**(7)**	**CO3**
b.	Explain how short channel and narrow width impacts the design performance of CMOS.	**(7)**	**CO2**
6. **Answer any one of the following-**			
a	Define impact ionization in MOS model and how scaling impacts the vertical and horizontal electric field?	**(7)**	**CO2**
b.	Derive the threshold model with and without body bias.	**(7)**	**CO2**
7. Answer any one of the following-			
a.	Make a comparison between MOS Model level1,2,3 with the help of mathematical models.	**(7)**	**CO5**
b.	Write a SPICE program for a NAND gate and define all global signals in the design.	**(7)**	**CO5**
8. Answer any one of the following-			
a	Draw a neat energy band diagrams for n-MOSFET and FINFET device. Compare the performance of both devices.	**(7)**	**CO4**
b	What is the importance of high k gate in MOS devices? Justify the statement.	**(7)**	**CO3**