

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA**(An Autonomous Institute Affiliated to AKTU, Lucknow)****MASTER OF COMPUTER APPLICATIONS (MCA)****(SEM: 1st Theory Examination (2020-2021))****SUBJECT NAME: COMPUTER SYSTEM ORGANIZATION****Time: 3 Hours****Max. Marks:100****General Instructions:**

- All questions are compulsory. Answers should be brief and to the point.
- This Question paper consists of02.....pages & ...8.....questions.
- It comprises of three Sections, A, B, and C. You are to attempt all the sections.
- **Section A** - Question No- 1 is objective type questions carrying 1 mark each, Question No- 2 is very short answer type carrying 2 mark each. You are expected to answer them as directed.
- **Section B** - Question No-3 is Long answer type -I questions with external choice carrying 6 marks each. You need to attempt any five out of seven questions given.
- **Section C** - Question No. 4-8 are Long answer type -II (within unit choice) questions carrying 10 marks each. You need to attempt any one part a or b.
- Students are instructed to cross the blank sheets before handing over the answer sheet to the invigilator.
- No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION – A

- 1. Attempt all the parts:** **[10×1=10]** CO
- | | | |
|--|-----|-----|
| a. $(125.5)_{10} = (?)_2 = (?)_8 = (?)_{16}$ | (1) | CO1 |
| b. What is r's and (r-1)'s complement? | (1) | CO1 |
| c. Using 10's complement, subtract 72532 - 3250 | (1) | CO1 |
| d. How many memory chips of (128 x 8) are needed to provide a memory capacity of 4096 x 16? | (1) | CO5 |
| e. Differentiate Computer Architecture and Computer Organization. | (1) | CO1 |
| f. Design half subtractor using NAND gates only. | (1) | CO1 |
| g. How can you make decoder to function as a demultiplexer? | (1) | CO1 |
| h. Gray code equivalent of $(1000)_2$ is | (1) | CO2 |
| i. How many address lines are needed to address each memory locations in a 2048x4 memory chip? | (1) | CO5 |
| j. In DMA, the data transfer is controlled by_____. | (1) | CO5 |
- 2. Attempt all the parts:** **[5×2=10]**
- | | | |
|---|-----|-----|
| a. Which addressing mode is used in an instruction of the form ADD R1,R2? | (2) | CO3 |
| b. Define opcode. | (2) | CO4 |
| c. Differentiate a level triggered from an edge triggered flip-flop. | (2) | CO1 |
| d. What is memory hierarchy? Why do we need it? | (2) | CO5 |
| e. What is the benefit of using a multiple –bus architecture compared to single-bus architecture? | (2) | CO3 |

SECTION – B

3. Answer any **five** of the following- [5×6=30] CO
- Discuss the Characteristic table and Excitation table of JK-Flip flop. (6) CO1
 - Define subroutine. How it is executed by the processor? What is the (6) CO3
 - What do you mean by Ripple counter? Design and explain Decade counter. (6) CO1
 - What do you mean by K-map? For function $F(A,B,C,D) = \sum(2,3,6,7,8,9,10,11)$, Draw the circuit diagram for the same. (6) CO1
 - What is Tri-state buffer? Design 4 bit Bus line using it. importance of subroutine parameters and data linkage? How it is established? (6) CO3
 - How many 128×8 RAM chips to provide a memory capacity of 2KB? How many address lines be required to access 2KB memory? How many lines must be decoded for chip select? Specify the size of decoder. (6) CO5
 - Explain with example the various modes of data transfer. (6) CO5

SECTION – C

- 4 Answer any **one** of the following- [5×10=50]
- Illustrate the working of a 4-bit bi-directional shift register. (10) CO1
 - Explain the operation of a T and JK master flip flop. (10) CO1
5. Answer any **one** of the following-
- Write short notes on followings (10) CO5
 - Daisy chaining priority.
 - Direct Memory Access.
 - Handshaking method for data transfer.
 - Associative Memory
 - Write a general algorithm and flow chart for addition and subtraction of two signed magnitude numbers. (10) CO4
6. Answer any **one** of the following-
- Explain the hardware organization of associative memory. Why associative memory is faster than other memories? Deduce the logic equation used to find the match in the associative memory. Explain how four-bit argument register is realized. (10) CO5
 - Explain Instruction cycle. Implement the RTL's of fetch phase. (10) CO3
7. Answer any **one** of the following-
- Explain different methods used for establishing the priority of simultaneous interrupts. (10) CO5
 - What is a microinstruction? Write a micro instruction code format and explain all the fields in it. (10) CO3
8. Answer any **one** of the following-
- What is serial communication system? How data is transmitted in synchronous serial communication system? (10) CO5
 - Consider a cache (M1) and memory (M2) hierarchy with the following characteristics: - (10) CO5
 M1: 16 K words, 50 ns access time M2: 1 M words, 400 ns access time. Assume 8 words cache blocks and a set size of 256 words with set associative mapping.
 (i) Show the mapping between M2 and M1.
 (ii) Calculate the Effective Memory Access time with a cache hit ratio of $h = 0.95$.