NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY GREATER NOIDA, GAUTAM BUDDH NAGAR

(An Autonomous Institute)

Affiliated to

Dr. A.P.J. ABDUL KALAM TECHNICAL UNIVERSITY UTTAR PRADESH, LUCKNOW

Evaluation Scheme & Syllabus

For

Bachelor of Technology

Electronics Engineering (VLSI Design and Technology)

Third Year

(Effective from the Session: 2026-27)

NOIDA INSTITUTE OF ENGINEERING & TECHNOLOGY, GREATER NOIDA
(An Autonomous Institute)

B. TECH (EE-VLSI)
Evaluation Scheme
SEMESTER V

S. No.	Subject Codes	Subject Name	Types of Subjects	Periods			Evaluation Schemes				End Semester		Total	Credit
				L	T	P	CT	TA	TOTAL	PS	TE	PE		
1	BECVL0501	CMOS Digital Integrated Circuit	Mandatory	3	1	0	30	20	50		100		150	4
2	BECVL0502	Static Timing Analysis	Mandatory	3	1	0	30	20	50		100		150	4
3	BCSCC0501Y	Design Thinking - II	Mandatory	2	0	0	60	40	100				100	2
4		Departmental Elective - II	Departmental Elective	3	0	0	30	20	50		100		150	3
5		Departmental Elective - III	Departmental Elective	3	0	0	30	20	50		100		150	3
6	BECVL0551	CMOS Digital Integrated Circuit Lab	Mandatory	0	0	4				50		50	100	2
7	BECVL0552	Static Timing Analysis Lab	Mandatory	0	0	2				25		25	50	1
8		Departmental Elective - II Lab	Departmental Elective	0	0	2				25		25	50	1
9	BECVL0555	System Verilog	Mandatory	0	0	6				150			150	3
10	BCSCC0552	Research Methodology, Ethics and Writing	Mandatory	0	0	2				50			50	1
11	BEC0559X	Internship - II	Mandatory	0	0	2				50			50	1
12	BVAC0551	Professional Practice & Employability - I	Compulsory Audit	0	0	6								NA
		*Massive Open Online Courses (For B.Tech. Hons. Degree)	*MOOC's											
			TOTAL	**14**	**2**	**24**	**180**	**120**	**300**	**350**	**400**	**100**	**1150**	**25**

*** List of MOOCs (Infosys Springboard) Based Recommended Courses for third year B. Tech Students**

S. No.	Subject Code	Course Name	University/ Industry Partner Name	No. of Hours	Credits
1.	BMC0104	Wireless Evolution and 4G LTE Overview	Infosys Wingspan (Infosys Springboard)	52h 4m	4
2.	BMC0118	Gen AI 101	NASSCOM	15h	1

PLEASE NOTE: -

- **A 3-4 weeks Internship shall be conducted during summer break after semester-IV and will be assessed during semester-V.**
- **Compulsory Audit (CA) Courses (Non-Credit - BVAC0551)**
  - All Compulsory Audit Courses (a qualifying exam) do not require any credit.
  - The Total and obtained marks are not added in the Grand Total.

Abbreviation Used:

L: Lecture, T: Tutorial, P: Practical, CT: Class Test, TA: Teacher Assessment, PS: Practical Sessional, TE: Theory End Semester Exam.
CE: Core Elective, OE: Open Elective, DE: Departmental Elective, PE: Practical End Semester Exam, CA: Compulsory Audit,
MOOCs: Massive Open Online Courses.

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B. TECH (EE-VLSI)
Evaluation Scheme
SEMESTER VI

S. No.	Subject Codes	Subject Name	Types of Subjects	Periods			Evaluation Schemes				End Semester		Total	Credit
				L	T	P	CT	TA	TOTAL	PS	TE	PE		
1	BECVL0601	Low Power VLSI Design	Mandatory	3	1	0	30	20	50		100		150	4
2	BECVL0602	VLSI Testing and Testability	Mandatory	3	1	0	30	20	50		100		150	4
3		Departmental Elective – IV	Departmental Elective	3	0	0	30	20	50		100		150	3
4		Departmental Elective – V	Departmental Elective	3	0	0	30	20	50		100		150	3
5		Open Elective – I	Open Elective	2	0	0	30	20	50		50		100	2
6	BECVL0653	Industrial PCB & Circuit Engineering Lab	Mandatory	0	0	4				50		50	100	2
7	BECVL0651	Low Power VLSI Design Lab	Mandatory	0	0	4				50		50	100	2
8		Departmental Elective - IV Lab	Departmental Elective	0	0	2				25		25	50	1
9	BECVL0654	AI & ML for VLSI (Workshop Mode)	Mandatory	0	0	6				50		100	150	3
10	BEC0659X	Applied Research with Mini Project	Mandatory	0	0	2				50			50	1
11	BVAC0651	Professional Practice & Employability - II	Compulsory Audit	0	0	6								NA
		*Massive Open Online Courses (For B.Tech. Hons. Degree)	*MOOC's											
			TOTAL	**14**	**2**	**24**	**150**	**100**	**250**	**225**	**450**	**225**	**1150**	**25**

*** List of MOOCs (Infosys Springboard) Based Recommended Courses for third year B. Tech Students**

S. No.	Subject Code	Course Name	University/ Industry Partner Name	No. of Hours	Credits
1.	BMC0116	Introduction to Generative AI – Artificial intelligence and Machine Learning	NASSCOM	15h	1
2.	BMC0103	Wireless 5G Overview	Infosys Wingspan (Infosys Springboard)	55h 44m	4
3.	BMC0084	Introduction to ML and AI	Infosys Wingspan (Infosys Springboard)	62h 54m	4

PLEASE NOTE: -

- **A 3-4 weeks Internship shall be conducted during summer break after semester-VI and will be assessed during Semester-VII**
- **Compulsory Audit (CA) Courses (Non-Credit - BVAC0651)**
  - All Compulsory Audit Courses (a qualifying exam) do not require any credit.
  - The Total and obtained marks are not added in the Grand Total.

Abbreviation Used:

L: Lecture, T: Tutorial, P: Practical, CT: Class Test, TA: Teacher Assessment, PS: Practical Sessional, TE: Theory End Semester Exam.
CE: Core Elective, OE: Open Elective, DE: Departmental Elective, PE: Practical End Semester Exam, CA: Compulsory Audit,
MOOCs: Massive Open Online Courses.

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List of Department Elective:

S. No.	Subject Code	Subject Name	Type of Subject	Bucket Name	Semester
1	BEC0512	Machine Learning	DE-II	AI & ML	V
2	BEC0514	Artificial Intelligence	DE-III		V
3	BEC0512ZP	AI & ML Lab	DE-II		V
4	BEC0612	Image Processing and Pattern Recognition	DE-IV		VI
5	BEC0615	ANN & Deep Learning	DE-V		VI
6	BEC0612P	Image Processing and Pattern Recognition Lab	DE-IV		VI
7	BEC0511	Embedded System Design	DE-II	Embedded & IoT	V
8	BEC0519	IoT Networks	DE-III		V
9	BEC0511P	Embedded System Design Lab	DE-II		V
10	BEC0616	Real Time Operating System	DE-IV		VI
11	BEC0617	Big Data Analytics for IoT & Internet of Everything	DE-V		VI
12	BEC0616P	Real Time Operating System Lab	DE-IV		VI
13	BECVL0511	Thin Film Transistor	DE-II	Semiconductor Devices and Display Technologies	V
14	BECVL0512	Compound Semiconductors	DE-III		V
15	BECVL0511P	Thin Film Transistor Lab	DE-II		V
16	BECVL0611	OLEDs & QLEDS	DE-IV		VI
17	BECVL0612	Emerging Memory Devices	DE-V		VI
18	BECVL0611P	OLEDS & QLEDS Lab	DE-IV		VI

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AICTE Guidelines in Model Curriculum:

A student will be eligible to get Under Graduate degree with Honours only, if he/she completes the additional MOOCs courses such as Infosys Springboard/NASSCOM/CISCO (as applicable) certifications, or any other online courses recommended by the Institute (Equivalent to 20 credits). During Complete B.Tech. Program Guidelines for credit calculations are as follows.

1. For 6 to 12 Hours =0.5 Credit
2. For 13 to18 =1 Credit
3. For 19 to 24 =1.5 Credit
4. For 25 to 30 =2 Credit
5. For 31 to 35 =2.5 Credit
6. For 36 to 41 =3 Credit
7. For 42 to 47 =3.5 Credit
8. For 48 and above =4 Credit

For registration to MOOCs Courses, the students shall follow Infosys Springboard/NASSCOM/CISCO (as applicable) registration details as per the assigned login and password by the Institute these courses may be cleared during the B. Tech degree program (as per the list provided). After successful completion of these MOOCs courses, the students shall provide their successful completion status/certificates to the Controller of Examination (COE) of the Institute through their coordinators/Mentors only.

The students shall be awarded Honours Degree as per following criterion.

i. If he / she secures 7.50 as above CGPA.
ii. Passed each subject of that degree program in the single attempt without any grace.
iii. Successful completion of MOOCs based 20 credits

Course Code: BECVL0501	Course Name: CMOS Digital Integrated Circuit	L	T	P	C
Course Offered in: B. Tech. Fourth Semester ECE / EE (VLSI)		**3**	**1**	**0**	**4**

Pre-requisite: Basis knowledge of MOSFET and Digital Electronics

Course Objectives:

The course aims to provide a comprehensive understanding of MOS transistor operation, CMOS inverter characteristics, and the design of CMOS-based combinational and sequential circuits. It enables students to apply dynamic logic design techniques for high-speed VLSI systems and develop an understanding of the organization and operation of semiconductor memories used in modern integrated circuits.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Explain the basics of MOS device and its current voltage characteristics.	K2
CO2	Explain MOS inverters and its static characteristics.	K3
CO3	Design of Combinational and Sequential MOS logic circuits.	K4
CO4	Explain and design dynamic logic circuits.	K4
CO5	Describe the concept of semiconductor memories.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	-	-	-	-	-	-	-	-	3	1	2
CO2	3	2	3	-	-	-	-	-	-	-	-	3	2	2
CO3	3	3	2	-	-	-	-	-	-	-	-	3	2	2
CO4	3	1	2	-	-	-	-	-	-	-	-	3	2	2
CO5	3	3	3	-	-	-	-	-	-	-	-	3	2	2

Course Contents / Syllabus

Unit 1	**VLSI Design Flow and CMOS fabrication**	**09 hours**

VLSI Design flow: VLSI Design flow & Y-Chart, MOS Structure, MOS System under external Bias, Structure and Operation of MOSFET, Basic MOS Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effect, MOSFET capacitances

Unit 2	**MOS inverter and Static Characteristics**	**09 hours**

Introduction, Resistive-load Inverter, Inverter with N-type MOSFET load, CMOS inverter: Circuit operation, DC transfer characteristics, Noise margin: calculation of VIL, VIH, Vth, Design of CMOS inverter, Supply voltage scaling, Switching characteristic: Delay time definition, calculation of delay times, Power dissipation of CMOS inverter.

Unit 3	**Combinational and sequential MOS logic circuits**	**09 hours**

Combinational MOS Logic Circuits with Depletion NMOS loads, CMOS Logic circuits – Realizing Boolean expressions using CMOS gates, Complex Logic circuits design, Design of Half Adder, Full Adder, CMOS Transmission Gates (Pass Gates) Sequential MOS Logic Circuits: Behavior of Bi-stable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D-latch, and edge triggered flip-flop.

Unit 4	**Dynamic logic Circuits**	**09 hours**

Introduction, Basic Principles of Pass Transistor Circuits, Synchronous dynamic circuit techniques: Dynamic Pass Transistor Circuits, CMOS Transmission Gate Logic, High performance Dynamic CMOS Logic Circuits: CMOS Domino Logic, charge sharing problem

Unit 5	**Introduction to Semiconductor memories and ASIC**	**09 hours**

Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells.

	Total Lecture Hours	**45 hours**

Textbook:		
		Authors Name
1. "CMOS Digital Integrated Circuits", TMH, 3rd Edition,		Kang, Leblebici
2. "Digital Integrated Circuit: A Design Perspective", PHI; Latest Edition,		Rabaey, Chandrakasan and Nikolic
3. "Principles of CMOS VLSI Design" Addison Wesley, Latest Edition.,		Weste and Eshraghian
Reference Books:		
		Authors Name
1. "CMOS VLSI Design".		Weste and Harris
2. "Essentials of VLSI Testing for digital, memory and mixed-signal VLSI Circuits", Kluwer Academic Publishers.		Bushnell and Agrawal
Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	**Unit 1** https://onlinecourses.nptel.ac.in/noc20_ee29/preview **Unit 2** https://www.youtube.com/watch?v=MuBiC9yz2fc **Unit 3** https://nptel.ac.in/courses/108/106/108106158 **Unit 4** https://www.youtube.com/watch?v=UuafwIJAKhY **Unit 5** https://www.youtube.com/watch?v=vD0sNigq1C	10Hrs 17Min 00Hrs 50Min 01Hrs 51Min 03Hrs 48Min 00Hrs 30Min
Web References		

Course Code: BECVL0502	Course Name: Static Timing Analysis	L	T	P	C
Course Offered in: B.Tech. EE (VLSI)		3	1	0	4

Pre-requisite: Defining clock characteristics, input/output delays, and path exceptions to ensure the design meets setup and hold times across all paths, Boolean Algebra, Sequential Circuits

Course Objectives:

The course aims to develop a strong understanding of timing analysis, delay mechanisms, and timing models in CMOS digital circuits. It enables students to apply Static Timing Analysis (STA) techniques, timing constraints, and industry-standard EDA tools for timing verification and closure. The course also prepares students to evaluate and optimize VLSI designs to meet sign-off quality requirements in advanced semiconductor technologies.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Explain the fundamentals of Static Timing Analysis (STA), timing paths, timing parameters, and timing models of combinational and sequential circuits in the CMOS design flow.	K2
CO2	Analyze interconnect parasitic, path delays, slack, and crosstalk effects, and perform setup and hold timing verification in digital VLSI circuits.	K4
CO3	Configure STA environments and timing constraints to perform setup, hold, recovery, removal, and multi-clock timing analysis for digital designs.	K4
CO4	Apply timing checks and timing exception techniques, including multicycle paths, false paths, and clock domain crossing analysis, to verify timing closure.	K4
CO5	Evaluate the impact of on-chip variations, power optimization techniques, and sign-off methodologies, and identify and resolve timing violations in advanced VLSI designs.	K4

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	2	-	-	-	-	-	-	-	3	3	2
CO2	3	3	2	2	-	-	-	-	-	-	-	3	3	2
CO3	3	3	2	2	-	-	-	-	-	-	-	3	3	2
CO4	3	3	3	2	-	-	-	-	-	-	-	3	3	2
CO5	3	3	3	2	-	-	-	-	-	-	-	3	3	2

Course Contents / Syllabus

Unit 1	**Introduction to STA**	**09 hours**

Definition and need of STA, STA In CMOS Digital Design flow, Limitations of STA, Propagation Delay, Slew of a Waveform, Skew between Signals, Min and Max Timing Paths, Operating Conditions, Timing Models of Combinational and Sequential Cells.

Unit 2	**Types of Delays in STA**	**09 hours**

Interconnect Parasitic - RLC for Interconnect, Interconnect Delay, Path Delay Calculations, Slack Calculations, Crosstalk Glitch Analysis, Crosstalk Delay Analysis, Positive and Negative Crosstalk, Timing Verification using Crosstalk and Delay-Setup and Hold Analysis

Unit 3	**Configuring the STA Environment**	**09 hours**

Configuring the STA Environment, Clock Uncertainty and Clock Latency, Generated Clock, Constraining input and output paths, Timing Path Groups, Design Rule Check (DRC Check), Virtual Clocks

Unit 4	**Timing Verification**	**09 hours**

Point-to-Point Specification, Path Segmentation, Setup and Hold Timing Check, Multicycle Path, False Path, Recovery and Removal Timing Check, Multiple Clocks

Unit 5	**Interface Analysis**	**09 hours**

On-Chip Verification, Time Borrowing, Clock Gating, Power Gating, Multi-Vt Cells, Sign-Off Methodology, Path Failing Timing.		
	Total Lecture Hours	**45 hours**
Textbook:		
		Authors Name
1. Static Timing Analysis Using Nanometer Designs", Springer Publication,		J. Bhasker, Rakesh Chadha
2. Constraining Designs for Synthesis and Timing Analysis,		Krish Tiwari
Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	https://www.youtube.com/watch?v=H34hLpUU9PA&list=PLLy_2iUCG87Bny6CcGkCanvlHuXwr4-_W&index=2	00Hrs 25Min
	https://www.youtube.com/watch?v=EPIu-6t_Ifg	01Hrs 51Min
	https://www.youtube.com/watch?v=akCyA4M2Zto&t=112s	03Hrs 48Min
	https://www.youtube.com/watch?v=lqIAUK9r14w	10Hrs 17Min
	https://www.youtube.com/watch?v=O7pN549AC14	00Hrs 30Min
	https://www.youtube.com/watch?v=ffJ6Z9pgvc4	01Hrs 51Min
	https://www.youtube.com/watch?v=3t8ndX2hqHA&t=148s	03Hrs 48Min
	https://www.youtube.com/watch?v=8w0Mu6qhqYE	01Hrs 25Min
	https://www.youtube.com/watch?v=O6HzFuOXvIg,	01Hrs 51Min
	https://www.youtube.com/watch?v=4NmrL30rx4k	03Hrs 48Min
Web References		

Course Code: BEC0512	Course Name: Machine Learning	L	T	P	C
Course Offered in: B.Tech. ECE/EE (VLSI)		3	0	0	3

Pre-requisite: Basics of mathematics and python programming

Course Objectives:

The course aims to introduce the fundamental concepts of machine learning, neural networks, and intelligent data analysis. It enables students to understand data representation, dimensionality reduction, probabilistic learning, search, and optimization techniques, and to apply machine learning algorithms for solving real-world data-driven problems and extracting meaningful insights.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
Course Outcome		
CO1	Describe the basic concepts of machine learning, statistics, and probability theory.	K2
CO2	Define and describe the Neurons, neural networks, and multilayer perceptron.	K2
CO3	Identify the dimensionality of data and reduces it using various mathematical concepts as well as describe the probabilistic learning.	K4
CO4	Describe and apply various search and optimization techniques to the raw data.	K3
CO5	Illustrate and apply various learning techniques.	K2

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	-	-	-	-	-	-	-	2	2	2	3
CO2	2	2	2	-	-	-	-	-	-	-	2	2	2	3
CO3	2	2	2	-	-	-	-	-	-	-	2	2	2	3
CO4	2	2	2	-	-	-	-	-	-	-	2	2	2	3
CO5	2	2	2	-	-	-	-	-	-	-	2	2	2	3

Course Contents / Syllabus

Unit 1	**Introduction to Machine Learning**	**09 hours**

Introduction, types of learning, History of ML, Introduction of Machine Learning Approaches, Introduction to Model Building, Sensitivity Analysis, Underfitting and Overfitting, Bias and Variance, Concept Learning Task, Find S Algorithms, Version Space and Candidate Elimination Algorithm, Inductive Bias, Issues in Machine Learning and Data Science Vs Machine Learning

Unit 2	**Neural Networks**	**09 hours**

Hebb's Rule, McCulloch and Pitts Neurons, Limitation of McCulloch and Pitts Neurons, The Perceptron, Linear separability, Linear Regression, Back propagation algorithm. The Multi-Layer Perceptron (MLP): MLP algorithm, Sequential and Batch training, Amount of training data, number of hidden layers, when to stop training. The network output and errors, Requirements of activation function.

Unit 3	**Dimensionality Reduction**	**09 hours**

Linear discriminant analysis, Principal Component analysis, Factor analysis, Independent Component analysis, locally linear embedding, ISOMAP Models: Gaussian Matrix Models, Nearest Neighbour methods. Support Vector Machine (SVM): Optimal separation, Kernels, SVM algorithm, Extensions of SVM.

Unit 4	**Optimization and Search**	**09 hours**

Gradient Descent, Batch GD, Mini-batch GD, SGD, Going Downhill, least square optimization, conjugate gradients, Exhaustive search, Greedy search, hill climbing. Evolutionary Learning: The genetic algorithm, Genetic operators, punctuated equilibrium, The Knapsack Problems.

Unit 5	**Reinforcement Learning**	**09 hours**

State and action spaces, the reward function, Markov chain decision process, Uses of Reinforcement Learning. Learning

with tree: Decision Tree, Classification and regression tree, Random Forest. Unsupervised Learning: The k-means algorithm, Vector quantization, The self-organization feature map, Simulated annealing.		
	Total Lecture Hours	**45 hours**
Textbook:		
	Authors Name	
1.“Machine Learning- An Algorithm Perspective”, CRC Press, 2nd edition.	Stephen Marsland	
2.“Introduction to Machine Learning (Adaptive Computation and Machine Learning)” The MIT Press 2004.	Ethem Alpaydin	
3.“Neural Networks”, Prentice Hall of India,	Siman Haykin	
4."Genetic Algorithms: Search, Optimization and Machine Learning",	Addison Wesley, D.E. Goldberg	
Reference Books:		
	Authors Name	
1. “Neural Networks”, Tata Mc Graw Hill,	Kumar Satish	
2. “Fuzzy Logic with Engineering Applications”	Wiley India.,Timothy J. Ross	
3. “Pattern Recognition and Machine Learning”, Berlin: Springer	Verlag.,Bishop, C.	
4. “An Introduction to Genetic Algorithms”, MIT Press, 2000.	Melanie Mitchell	
Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	https://www.youtube.com/watch?v=T3PsRW6wZSY&list=PLJ5C_6qdAvBGaabKHmVbtryZW9KpICiHC	01Hrs 51Min
Web References		

Course Code: BEC0511	Course Name: Embedded System Design	L	T	P	C
Course Offered in: B.Tech. EE (VLSI)		3	0	0	3

Pre-requisite: Knowledge of Microprocessor and Microcontroller.

Course Objectives:

The course aims to provide a strong foundation in embedded system design, ARM Cortex-M4 architecture, and programming using the STM32F401 platform. It enables students to develop embedded applications through hardware interfacing and ARM programming, while introducing the concepts of embedded Linux and Linux kernel architecture for modern embedded systems.

Course Outcome: After completion of the course, the student will be able to

Course Outcome		Bloom's Level
CO1	Compute the design considerations of embedded systems.	K3
CO2	Apply the knowledge to learn STM32F401 for various application.	K4
CO3	Analyze the Architecture of ARM CORTEX-M4 processor.	K4
CO4	Implement the programming techniques for ARM processor.	K3
CO5	Evaluate the concept of embedded Linux and kernel architecture.	K4

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2	-	-	-	-	-	-	2	2	3	2
CO2	3	2	3	2	-	-	-	-	-	-	2	3	3	2
CO3	3	3	2	2	-	-	-	-	-	-	2	3	3	2
CO4	3	2	3	2	-	-	-	-	-	-	2	3	3	2
CO5	3	3	2	2	-	-	-	-	-	-	2	3	3	2

Course Contents / Syllabus

Unit 1	Introduction to Embedded Systems	09 hours

Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems, Design Considerations of Embedded Systems.

Unit 2	STM32F401	09 hours

STM32F401 Nucleo Board, Interfacing with Analog World, Output Devices, Sensors and Actuators, Interfacing with 7 segment LED and LCD Displays, Interfacing with Temperature Sensor and LDR Light Sensor, Speed Control of DC Motor.

Unit 3	Arm Architectures and Processors	09 hours

Key features of Arm architectures and processors, Structure and purpose of specific registers in the Arm Cortex-M4 processor, Interrupts: Nested Vectored Interrupt Controller (NVIC), Wakeup Interrupt Controller (WIC), Memory Protection Unit (MPU), Bus Interconnect and Debug System and Low Power Features.

Unit 4	Introduction to Arm Cortex	09 hours

M4 Programming, Compare the C and Assembly programming languages, C as Implemented in Assembly Language, Benefits and drawbacks of high-level and low-level programming, Introduction to the Mbed Platform and CMSIS, Mbed platform and its importance.

Unit 5	History of Embedded Linux	09 hours

Semiconductor Memories: Basic concepts and hierarchy of Memory, Memory elements-ROM, RAM, comparison, Designing and circuit implementation using programmable logic devices: PROM, PAL, PLA, Introduction of CPLD and FPGA.

Total Lecture Hours	45 hours

Textbook:	
	Authors Name
1. "ARM system developers guide", Elsevier, Morgan Kaufman publishers, 2008.,	Andrew N Sloss,Dominic Symes Chris Wright
2. The Definitive Guide to the ARM Cortex-M3, 2nd Edition, Newnes, 2009,	Joseph Yiu
3. Embedded Linux System Design and Development,	P. Raghavan, Amol Lad, Sriram

Reference Books:	
	Authors Name
1. Introduction to Embedded Systems‖, Tata McGraw Hill Education Private Limited, 2009.	Shibu K V
2. "Embedded Systems: Architecture, Programming and design, Second Edition, Tata McGraw Hill publisher, 2010.	Raj Kamal
3. "An Embedded Software Primer", Pearson Education.	David E. Simon
4. ARM System-on-Chip Architecture, Second Edition, Pearson, 2015,	Steve Furber

Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	https://onlinecourses.nptel.ac.in/e-learning/preview/noc22_cs93 https://www.arm.com/glossary/embedded-system-design https://www.coursera.org/specializations/advanced-embedded-linux-development	00Hrs 25Min 01Hrs 51Min 03Hrs 48Min
Web References		

Course Code: BECVL0511	Course Name: Compound Semiconductor	L	T	P	C
Course Offered in: B.Tech. EE (VLSI)		3	0	0	3

Pre-requisite: Basic knowledge of Semiconductor materials.

Course Objectives:

This course offers an in-depth exploration of compound semiconductors. Focusing on the unique properties, materials, and applications that distinguish them from traditional elemental semiconductors. Students will delve into the fabrication processes, device physics, and emerging technologies associated with compound semiconductors

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Comprehensive Understanding of Compound Semiconductor Materials	K2
CO2	Device Physics of Compound Semiconductor	K3
CO3	Fabrication Techniques and Processes:	K4
CO4	Applications in Electronic and Optoelectronic Devices	K3
CO5	Emerging Technologies and Trends in Compound Semiconductors	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	1	2	2		-	-	-	-	-	-	2	2	1
CO2	3	1	2	1	1	-	-		-	-	-	2	2	1
CO3	3	1	2	2	1	-	-	--	-	-	-	2	2	1
CO4	3	1	3	2	1	-	-	-	-	-	-	2	2	1
CO5	3	1	2	2	1	-	-	-	-	-	-	2	2	1

Course Contents / Syllabus

Unit 1	**Introduction to Compound Semiconductors**	**09 hours**

Overview of compound semiconductors and their significance, Historical context and evolution of compound semiconductor technologies Introduction to key compound semiconductor materials.

Unit 2	**Properties and Device Physics of Compound Semiconductors**	**09 hours**

Crystal structures and properties of compound semiconductors, Comparison with elemental semiconductors. Device physics principles specific to compound semiconductors. High-speed transistors and integrated circuits.

Unit 3	**Principles of Compound Semiconductor Optoelectronics**	**09 hours**

Principles and applications of optoelectronic devices using compound semiconductors. Lasers, photodetectors, and light-emitting diodes (LEDs).

Unit 4	**Fabrication Technology of Compound Semiconductors**	**09 hours**

Epitaxial growth techniques for compound semiconductors. Lithography and etching processes specific to compound semiconductors.

Unit 5	**Applications and Emerging Trends in Compound Semiconductors**	**09 hours**

Applications of compound semiconductors in high-frequency devices, Microwave transistors and communication devices. Latest developments and trends in compound semiconductor technology.

	Total Lecture Hours	**45 hours**

Textbook

	Author
1. KehYungCheng.III-VCompoundSemiconductorsandDevices.Springer,2020.	Keh Yung Cheng
2. Udo W.Pohl. Epitaxy of Semiconductors: Physics and Fabrication of Heterostructures. Springer, 2020	Udo W. Pohl.

Reference Books:

Book Title with publication agency & year	Author
1. Optoelectronic devices and systems.PHILearningPvt.Ltd.,2014	Gupta, S
2. Birtalan, Dave. Optoelectronics. CRC Press, 2018	Birtalan, Dave.

Self-Study Content Links:		Duration (in Hrs)
MOOCs		
Video Lectures	https://www.youtube.com/watch?v=xBYhHC8_A6o	00Hrs 25Min
	https://www.youtube.com/watch?v=cNN_tTXABUA	01Hrs 51Min
	https://www.youtube.com/watch?v=sLW1TptEJBQ	03Hrs 48Min
	https://www.youtube.com/watch?v=9zOo4JkZgSI	10Hrs 17Min
	https://www.youtube.com/watch?v=Anj8OYXAY20	00Hrs 55Min
Web References		

Course Code:BEC0514	Course Name: Artificial Intelligence	L	T	P	C
Course Offered in: B. Tech ECE/ EE (VLSI)		3	0	0	3

Pre-requisite: Knowledge of Microprocessor and Microcontroller.

Course Objectives: Basic knowledge of AI and Machine Learning Concepts

This course introduces the fundamental concepts, principles, and evolution of Artificial Intelligence, along with problem-solving and reasoning techniques used in intelligent systems. It covers knowledge representation, learning methodologies, expert systems, search strategies, and evolutionary algorithms for developing AI-based solutions to complex real-world problems.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Elaborate historical perspective of AI and its foundations.	K2
CO2	Apply principles of AI toward problem solving and drawing inference thereof.	K3
CO3	Describe perception, knowledge representation, and different learning techniques.	K2
CO4	Implement architecture of knowledge-Based System, Rule-based systems, and other expert systems.	K3
CO5	Apply evolutionary computational algorithms and different search algorithms.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2	-	-	-	-	-	-	2	2	3	2
CO2	3	2	3	2	-	-	-	-	-	-	2	3	3	2
CO3	3	3	2	2	-	-	-	-	-	-	2	3	3	2
CO4	3	2	3	2	-	-	-	-	-	-	2	3	3	2
CO5	3	3	2	2	-	-	-	-	-	-	2	3	3	2

Course Contents / Syllabus

Unit 1	**Introduction to Artificial Intelligence**	**09 hours**

Historical developments of Artificial Intelligence, Well-defined learning problems, Designing a Learning System. Intelligent Agents: Characteristics of Intelligent Agents, Typical Intelligent Agents, Problem Solving Approach to Typical AI problems.

Unit 2	**Problem Solving Methods**	**09 hours**

Search Strategies: Uninformed Search Strategies: DFS, BFS, Informed Search Strategies: Local search algorithms and optimistic problems, adversarial Search, Search for games, minimax, Alpha - Beta pruning, Heuristic Search techniques, Hill Climbing, Best-first search, Iterative deepening Heuristic Search and A*.

Unit 3	**Logic and Knowledge Representation**	**09 hours**

Introduction of Logic, Propositional Logic Concepts, Semantic Tableaux and Resolution, Propositional logic, FOPL, Semantic Tableaux and Resolution in FOPL, Logic Programming in Prolog. Production systems and rules for some AI problems: Water Jug Problem, Missionaries-Cannibals Problem, n-Queen problem, monkey banana problem, Travelling Salesman Problem. Knowledge representation, semantic nets, partitioned nets, parallel implementation of semantic nets. Frames, Common Sense reasoning and thematic role frames.

Unit 4	**Expert System**	**09 hours**

Architecture of knowledge-Based System, Rule-based systems, Forward and Backward Chaining, Frame Based systems. Architecture of Expert System, Forward & Backward chaining, Resolution, Probabilistic reasoning, Utility theory, Hidden Markov Models (HMM), Bayesian Networks.

Unit 5	**Planning and Uncertainty**	**09 hours**

Planning with state Space Search, Conditional Planning, Continuous planning, Multiagent Planning, Forms of learning, inductive learning, Reinforcement Learning, learning decision trees, Neural Net learning, and Genetic learning. Probabilistic Methods, Bayesian Theory, Dempster Shafer Theory, Bayes Network.

Evolutionary computation: Swarm Intelligence, ant colony optimization. Case Study: Health Care, ECommerce, Smart Cities.		
		Total Lecture Hours **45 hours**
Textbook:		
		Authors Name
1.“Artificial Intelligence–A Modern Approach”, Pearson Education,4th Edition.		Stuart Russell, Peter Norvig
2.“Artificial Intelligence”, McGraw-Hill 3rd Edition 2010.		Elaine Rich and Kevin Knight
Reference Books:		
		Authors Name
1.“Artificial Intelligence”, Pearson Education Inc., Third edition, Patrick Henry Winston		Patrick Henry Winston
Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	https://nptel.ac.in/courses/106102220	03Hrs 48Min
Web References		

Course Code: BEC0519	Course Name: IoT Networks	L	T	P	C
Course Offered in: B. Tech ECE / EE (VLSI)		3	0	0	3

Pre-requisite: Basics of IoT and its Protocols

Course Objectives: Basic knowledge of AI and Machine Learning Concepts

The course aims to provide a comprehensive understanding of modern networking technologies, Software-Defined Networking (SDN), Network Function Virtualization (NFV), and Internet of Things (IoT) architectures. It enables students to apply virtualization concepts in cloud environments and evaluate network security mechanisms for designing secure, scalable, and efficient communication systems.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Explain the concept of modern networking and their types.	K2
CO2	Analyze the SDN and NFV related networks.	K4
CO3	Describe the various components of IoT Enabled Things.	K2
CO4	Explain the concept of virtual machines and their network functions.	K2
CO5	Describe the various requirements of security	K2

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	-	-	-	-	-	-	-	2	2	2	3
CO2	3	3	2	-	-	-	-	-	-	-	2	2	2	3
CO3	3	3	2	-	-	-	-	-	-	-	2	2	3	3
CO4	3	3	2	-	-	-	-	-	-	-	2	2	3	3
CO5	3	3	2	-	-	-	-	-	-	-	2	2	3	3

Course Contents / Syllabus

Module 1	**Modern Networking**	**09 hours**

Cloud Computing, Internet of Things - Types of Networks and Internet Traffic, Demand: Big Data, Cloud Computing and Mobile Traffic Requirements: QoS and QoE Routing Congestion Control, SDN and NFV, Modern Networking Elements

Module 2	**Software Defined Networks**	**09 hours**

Network Requirements, The SDN Approach, SDN and NFV Related Standards, SDN Data Plane, Open Flow Logical Network Device, Open Flow Protocol, SDN Control Plane Architecture, REST API, SDN Application Plane Architecture

Module 3	**IoT Components**	**09 hours**

The IoT Era, Scope of the Internet of Things, Components of IoT-Enabled Things, loT World Forum Reference Model, ITU-T IoT Reference Model, Cisco IoT System, Io Bridge, SDN and NFV over IoT Deployment

Module 4	**Virtualization**	**09 hours**

Background and Motivation for NFV, Virtual Machines, NFV Concepts, NFV Reference Architecture, NFV Infrastructure, Virtualized Network Functions, NFV Management and Orchestration, NFV Use Cases, SDN and NFV

Module 5	**IoT Security**	**09 hours**

Security Requirements, SDN Security, NFV Security, ETSI Security Perspective, IoT Security, The Patching Vulnerability, IoT Security and Privacy Requirements Defined by ITU-T, An IoT Security Framework, The Impact of the New Networking on IT Careers

	Total Lecture Hours	**45 hours**

Textbook:

	Authors Name
1."Foundations of Modern Networking: SDN, NFV, QoE, IoT, and Cloud", Addison-Wesley 2015.,	William Stallings

2.“SDN and NFV Simplified: A Visual Guide to Understanding Software Defined Networks and Network Function Virtualization”,	Jim Doherty
Reference Books:	
	Authors Name
1.“Software Defined Networks: A Comprehensive Approach”	Paul Goransson Chuck Black
2.“Network Function virtualization with a touch of SDN”	Paresh Shah, Syed Farrukh Hassan, Rajendra Chayapathi

Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	https://onlinecourses.nptel.ac.in/noc19_cs65/unit?unit=15&lesson=16	00Hrs 25Min
	https://onlinecourses.nptel.ac.in/noc19_cs65/unit?unit=75 &lesson=76	01Hrs 51Min
	https://onlinecourses.nptel.ac.in/noc21_cs20/unit?unit=49&lesson=53	03Hrs 48Min
	https://www.youtube.com/watch?v=VISUJUR1uV4	10Hrs 17Min
	https://www. business. att.com/learn/tech-advice/the-security-benefits-of-software-defined-networking--sdn-.html	01Hrs 48Min
Web References		

Course Code: BECVL0512	Course Name: Thin Film Transistor	L	T	P	C
Course Offered in: B.Tech. EE (VLSI)		3	0	0	3

Pre-requisite: Knowledge of Semiconductor Devices & Basic Microfabrication.

Course Objectives:

The course aims to provide a strong foundation in the principles, architectures, fabrication technologies, and device physics of Thin-Film Transistors (TFTs). It enables students to analyze TFT characteristics, design TFT-based analog and digital circuits, and explore their applications in flexible electronics, display technologies, and emerging large-area electronic systems.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Explain the evolution, classification, architectures, substrate technologies, and contact engineering aspects of Thin-Film Transistors (TFTs) and compare them with bulk MOSFET technologies.	K2
CO2	Explain the evolution, classification, architectures, substrate technologies, and contact engineering aspects of Thin-Film Transistors (TFTs) and compare them with bulk MOSFET technologies.	K2
CO3	Apply TFT device physics and transport models to evaluate electrical characteristics, non-idealities, and performance limitations in advanced TFT structures.	K3
CO4	Design and analyze reliable digital and analog TFT-based circuits considering degradation mechanisms, charge trapping, and self-heating effects.	K4
CO5	Evaluate TFT applications in display backplanes, flexible electronics, monolithic 3D integration, neuromorphic systems, and emerging large-area electronic systems.	K4

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	-	-	-	-	-	-	-	-	2	2	2
CO2	2	2	2	-	-	-	-	-	-	-	-	2	3	2
CO3	2	2	2	-	-	-	-	-	-	-	-	2	3	2
CO4	2	2	2	-	-	-	-	-	-	-	-	2	3	3
CO5	2	2	2	-	-	-	-	-	-	-	-	2	3	3

Course Contents / Syllabus

Unit 1	**Thin Film Transistor Material**	**09 hours**

Evolution of Thin-Film Transistors (TFTs) versus Bulk MOSFETs, Classification of TFTs: a-Si:H, Poly-Si/LTPS, IGZO, and Organic TFTs (OTFTs), Device Architectures: Staggered and Coplanar Structures, Top-Gate and Bottom-Gate Configurations Substrate Materials: Glass, Polyimide, Flexible Plastics and Thermal Constraints, Energy Band Diagrams, Work Function Matching, and Contact Resistance at Source/Drain Interfaces

Unit 2	**Thin-Film Fabrication and Patterning Processes**	**09 hours**

Thin-Film Deposition Techniques: LPCVD, PECVD, PVD, and Sputtering, Solution-Processed and Vacuum-Deposited Organic Films. Low-Temperature Crystallization Techniques: Excimer Laser Annealing (ELA) and Solid-Phase Crystallization (SPC), Photolithography on Flexible Large-Area Substrates, Wet and Dry Etching Techniques, Alternative Patterning Techniques: Inkjet Printing and Roll-to-Roll Processing.

Unit 3	**Device Physics and Transport Modeling**	**09 hours**

Operating Principles of Accumulation-Mode and Inversion-Mode TFTs, Density of States (DOS): Tail States, Deep States, and Grain Boundary Trap Models, Transport Mechanisms: Hopping Conduction, Multiple Trap and Release (MTR), and Thermionic Emission, Modeling of Non-Ideal Effects: Short Channel Effects (SCE), Drain-Induced Barrier Lowering (DIBL), and Kink Effects in Poly-Si TFTs		
Unit 4	**Device Reliability and TFT Circuit Design**	**09 hours**
Reliability Issues: NBTI/PBTI, Hot Carrier Degradation, Charge Trapping, and Self-Heating Effects, Digital TFT Circuits: Static and Dynamic TFT Inverters, Pseudo-CMOS Logic, Combinational Logic Gates, and Shift Registers, Analog TFT Circuits: Current Mirrors, Differential Amplifiers, and Operational Amplifiers using Unipolar/Oxide TFTs		
Unit 5	**Display Backplanes and Monolithic 3D Integration**	**09 hours**
AMLCD and AMOLED Pixel Circuit Design, AMOLED Compensation Techniques for Threshold Voltage Non-Uniformity Flexible Sensor Arrays, RFID Tags, and Printed Smart Systems, Monolithic 3D VLSI Integration using BEOL-Compatible TFTs, Applications in 3D NAND Flash Memory and Neuromorphic Synaptic Arrays		
	Total Lecture Hours	**45 hours**

Textbook:

	Authors Name
1. Organic Field-Effect Transistors, Springer.,	Yoshihiro Iwasa
2. Technology and Applications of Amorphous Silicon, 1st Edition, Springer, 2000.,	R. A. Street
3. OLED Display Fundamentals and Applications, 2nd Edition, Wiley, 2017,	Takatoshi Tsujimura

Reference Books:

	Authors Name
1. Flexible Electronics: Materials and Applications, 1st Edition, CRC Press, 2017.	Norbert Münzenrieder and Giacomo Indiveri
2. Thin-Film Transistors, 1st Edition, Marcel Dekker, 2003.	Cherie R. Kagan and Paul Andry

Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	https://youtu.be/YLczBemZpaE?si=wJCdoUed7epj52H9	01Hrs 25Min
	https://youtu.be/ezTRtlLziow?si=YfFX-VLb2OY1aqYX	01Hrs 51Min
	https://youtu.be/0FXg3P10Pck?si=-BaOiteRGMPkuL0G	03Hrs 48Min
	https://youtu.be/695JWL5j6Jw?si=hvSpiJC5QVFQb1BQ	10Hrs 17Min
	https://youtu.be/SLZMSqeqfQ4?si=SyTXdyvpvsZ5ypuh	00Hrs 45Min
Web References		

LAB Course Code: BECVL0551	Course Name: CMOS Digital Integrated Circuit Lab	L	T	P	C
Course Offered in: B. Tech. Fourth Semester ECE / EE (VLSI)		0	0	4	2

Pre-requisite: Basis knowledge of MOSFET and Digital Electronics

Course Objectives:

The course aims to develop practical skills in the simulation and analysis of CMOS devices and digital circuits. It enables students to design, verify, and evaluate CMOS inverters, combinational logic circuits, and SRAM cells using industry-standard simulation tools while applying advanced CMOS design techniques.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Simulate and analyze ID–VGS and ID–VDS characteristics of NMOS and PMOS transistors and extract device parameters.	K3
CO2	Analyze the voltage transfer characteristics (VTC) of NMOS and CMOS inverters and determine key parameters such as VOH, VOL, VIH, VIL, and Vth.	K4
CO3	Design and simulate CMOS logic circuits including NOR gates, half adder, and full adder, and verify their truth tables.	K3
CO4	Design and evaluate advanced CMOS circuits such as pass transistor logic, transmission gates.	K4
CO5	Simulate and analyze 6T SRAM cell for functionality and Performance.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	-	3	-	-	-	-	-	-	3	3	3
CO2	3	2	3	-	3	-	-	-	-	-	-	2	3	2
CO3	3	3	2	-	3	-	-	-	-	-	-	3	3	2
CO4	3	1	2	-	3	-	-	-	-	-	-	2	3	3
CO5	3	3	3	-	3	-	-	-	-	-	-	2	3	3

List Of Practical's (Indicative & Not Limited To)

S. No.	Objective	CO
1.	Introduction of Cadence tool/Micro wind, Schematic Editor, Layout Editor.	**CO1**
2.	Simulation and Analysis of I_D-V_{GS} and I_D-V_{DS} characteristics of NMOS and PMOS transistors.	**CO1**
3.	To obtain the NMOSFET parameters: kn, vto, vt, γ.	**CO1**
4.	To analyse the voltage transfer characteristics (VTC) of resistive-load NMOS inverter and calculate VOH, VOL, VIH, VIL and Vth.	**CO2**
5.	To analyse the voltage transfer characteristics (VTC) of CMOS inverter.	**CO2**
6.	To obtain the CMOS Inverter parameters: VOH, VOL, VIH, VIL and Vth.	**CO2**
7.	To simulate the CMOS 2 input NOR gates and verify the truth tables:	**CO3**
8.	To simulate the CMOS 2 input NOR gates and verify the truth tables:	**CO3**
9.	To simulate the CMOS Half Adder Circuit and verify the truth tables:	**CO3**
10.	To simulate the CMOS full Adder Circuit and verify the truth tables:	**CO3**
11.	Design and simulation of a Pass Transistor.	**CO4**
12.	Design and simulation of Transmission Gate logic.	**CO4**
13.	To design and simulate a 6-transistor SRAM cell**.**	**CO5**

Total Hours: 30 hrs.

LAB Course Code: BECVL0552	LAB Course Name: STA Lab	L	T	P	C
Course Offered in: B. Tech. EE (VLSI)		0	0	2	1

Pre-requisite: Basics of Digital Electronics, VLSI Design Flow

Course Objectives:

This course provides a comprehensive understanding of Static Timing Analysis (STA) and timing verification techniques using industry-standard EDA tools. It covers timing constraints, setup and hold analysis, clock uncertainties, advanced sign-off methodologies, and timing closure techniques to ensure reliable and high-performance VLSI circuit design.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Apply basic Static Timing Analysis concepts using industry-standard STA tools such as Synopsys Prime-Time and Cadence Tempus to load design libraries, define timing constraints, and perform setup/hold timing analysis.	K2
CO2	Analyze timing behavior of synchronous digital circuits by evaluating setup/hold violations, clock skew, clock uncertainty, clock gating, and timing exception constraints such as false paths and multicycle paths.	K4
CO3	Evaluate advanced STA methodologies including Multi-Mode Multi-Corner (MMMC) analysis, On-Chip Variation (OCV/AOCV/SOCV), and Clock Domain Crossing (CDC) verification for sign-off timing validation.	K4
CO4	Perform timing closure and Engineering Change Order (ECO) optimization techniques to resolve timing violations and improve overall circuit performance, reliability, and timing convergence.	K4

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	-	3	-	-	-	-	-	2	2	3	2
CO2	2	2	2	-	3	-	-	-	-	-	2	2	3	2
CO3	2	2	2	-	3	-	-	-	-	-	2	2	3	2
CO4	2	2	2	-	3	-	-	-	-	-	2	2	3	2

List Of Practical's (Indicative & Not Limited To)

S. No.	Objective	CO
1.	Introduction to Synopsys PrimeTime/Cadence Tempus Flow: Loading libraries, netlists, and running basic STA reports.	**CO1**
2.	To Simulate Clock and I/O Constraint Definition using create_clock, set_input_delay, and set_output_delay.	**CO1**
3.	To Simulate Setup Time Analysis and Critical Path Identification.	**CO1**
4.	To Simulate Hold Time Analysis and Hold Violation Fixing using Buffer Insertion.	**CO2**
5.	To Simulate the analysis of Clock Skew and Clock Uncertainty on Timing Performance.	**CO2**
6.	To Simulate the timing Exception Analysis using set_false_path.	**CO2**
7.	To Simulate Multicycle Path Timing Analysis using set_multicycle_path.	**CO3**
8.	To Simulate Clock Gating Timing Verification and Enable Signal Analysis.	**CO3**
9.	To determine and simulate multi-Mode Multi-Corner (MMMC) Timing Analysis across PVT Corners.	**CO3**

10.	To determine On-Chip Variation (OCV/AOCV/SOCV) and Timing Derating Analysis.	**CO4**
11.	To analyse Clock Domain Crossing (CDC) Analysis using Synchronizer Circuits.	**CO4**
12.	To Determine timing Closure and Engineering Change Order (ECO) based Timing Optimization	**CO4**
		Total Hours: 15 hrs.

LAB Course Code: BEC0512ZP	LAB Course Name: AI & ML Lab	L	T	P	C
Course Offered in: B. Tech. EE (VLSI)		0	0	2	1

Pre-requisite: Basics of Python

Course Objectives:

Understand and implement fundamental AI search algorithms for problem-solving. Analyze and solve AI-based problems using suitable intelligent techniques. Apply chaining and inference algorithms using programming tools such as Python. Implement and evaluate Machine Learning algorithms for predictive and analytical tasks. Develop AI and ML solutions for real-world applications and challenges.

Course Outcome: After completion of the course, the student will be able to		Bloom's Level
CO1	Implement the blind search algorithm.	K3
CO2	Implement the different AI based problem	K3
CO3	Apply various chaining algorithm in AI using python/Open CV	K3
CO4	Apply appropriate data sets to the Machine Learning algorithms.	K3
CO5	Identify and apply Machine Learning algorithms to solve real world problems.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	-	3	-	-	-	-	-	2	2	2	3
CO2	2	2	2	-	3	-	-	-	-	-	2	2	2	3
CO3	2	2	2	-	3	-	-	-	-	-	2	2	2	3
CO4	2	2	2	-	3	-	-	-	-	-	2	2	2	3
CO5	2	2	2	-	3	-	-	-	-	-	2	2	2	3

List Of Practical's (Indicative & Not Limited To)

S. No.	Objective	CO
1.	Implementation of Python basic Libraries such as Math, Numpy and Scipy.	CO1
2.	Implementation of Python Libraries for ML application such as Pandas and Matplotlib.	CO1
3.	Creation and loading different datasets in Python.	CO1
4.	Familiarizing with Anaconda for importing modules and dependencies for ML.	CO1
5.	Familiarizing with Jupyter for importing Modules and dependencies for ML.	CO1
6.	Write a python program to compute Mean, Median.	CO1
7.	Write a python program to compute Mode, Variance and Standard Deviation using Datasets.	CO1
8.	Write a Program to Implement Breadth First Search using Python.	CO1
9.	Write a Program to Implement Depth First Search using Python.	CO1
10.	Write a program to implement Hill Climbing Algorithm using Python.	CO2
11.	Write a program to implement Tic-Tac-Toe Game using Python.	CO2
12.	Write a Program to implement Game Playing Algorithms: Minimax.	CO2
13.	Write a Program to Implement A* Algorithm using Python.	CO2
14.	Write a Program to implement Game Playing Algorithms: Alpha Beta Pruning.	CO2

15.	Write a Program to implement Chatbot in Python.	**CO2**
16.	Write a Program to Implement Missionaries Cannibals Problems using Python.	**CO2**
17.	Write a Program to Implement 8-Puzzle Problem using Python.	**CO2**
18.	Write a program to solve water jug problem using Python.	**CO2**
19.	Write a program to solve Monkey banana problem using Python.	**CO2**
20.	Write a program to Implement N-Queens Problem Using Python.	**CO2**
21.	Write a program to Implement of Traveling Salesman using Python.	**CO2**
22.	Write a Program to Implement Tower of Hanoi using Python.	**CO2**
23.	Write a Program to Implement Forward Chaining.	**CO3**
24.	Write a Program to Implement Backward Chaining	**CO3**
25.	Implement the S algorithm for finding the most specific hypothesis based on a given set of training data samples. Read the training data from a .csv file.	**CO4**
26.	For a given set of training data examples stored in a .csv file, implement and demonstrate the Candidate Elimination algorithm to output a description of the set of all hypotheses consistent with the training examples.	**CO4**
27.	Build an Artificial Neural Network by implementing the Back propagation algorithm and test the same using appropriate data sets.	**CO4**
28.	Implement the non-parametric Locally Weighted Regression algorithm in order to fit data points. Select appropriate data set for your experiment and draw graphs.	**CO4**
29.	Implement the S algorithm for finding the most specific hypothesis based on a given set of training data samples. Read the training data from a .csv file.	**CO4**
30.	Write a program to implement the naïve Bayesian classifier for a sample training data set stored as a .csv file. Compute the accuracy of the classifier, considering few test data sets.	**CO5**
31.	Write a program to construct a Bayesian network considering medical data. Use this model to demonstrate the diagnosis of heart patients using standard Heart Disease Data Set. You can use Java/Python ML library classes/API.	**CO5**
32.	Apply EM algorithm to cluster a set of data stored in a .csv file. Use the same data set for clustering using kMeans algorithm. Compare the results of these two algorithms and comment on the quality of clustering. You can add Java/Python ML library classes/API in the program.	**CO5**
33.	Write a program to implement k-Nearest Neighbor algorithm to classify the iris data set. Print both correct and wrong predictions. Java/Python ML library classes can be used for this problem.	**CO5**
34.	Write a program to demonstrate the working of the decision tree based ID3 algorithm. Use an appropriate data set for building the decision tree and apply this knowledge to classify a new sample.	**CO5**
		Total Hours: 15 hrs.

LAB Course Code: BEC0511P	LAB Course Name: Embedded System Design Lab	L	T	P	C
Course Offered in: B. Tech. EE (VLSI)		0	0	2	1

Pre-requisite: Basics of Microprocessor and Microcontroller

Course Objectives:

The course aims to develop practical skills in programming ARM-based microcontrollers using the Freedom KL25Z development board. It enables students to design, implement, and test embedded systems using commercial development tools, APIs, and software frameworks to meet real-world application requirements.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Write a program for ARM based microcontroller.	K3
CO2	Analyze Freedom KL25Z board to build a system.	K4
CO3	Build an ARM-based embedded system, and program to satisfy given user specifications.	K3
CO4	Use commercial tools to develop ARM-based embedded systems.	K3
CO5	Use commercial API and tools to accelerate the development cycle of ARM-based embedded systems.	K4

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	-	2	-	-	-	-	-	2	2	2	2
CO2	2	2	2	-	2	-	-	-	-	-	2	2	2	2
CO3	2	2	2	-	2	-	-	-	-	-	2	2	2	2
CO4	2	2	2	-	2	-	-	-	-	-	2	2	2	2
CO5	2	2	2	-	2	-	-	-	-	-	2	2	2	2

List Of Practical's (Indicative & Not Limited To)

S. No.	Objective	CO
1.	Describe architecture and Pin diagram of Freedom KL25Z board.	**CO2**
2.	Write and compile the code to perform the arithmetic operations in ARM thumb instruction set.	**CO1**
3.	Write and compile the code to perform logical operations in ARM thumb instruction set.	**CO3**
4.	Write and compile code to perform Shift operations in ARM instruction set.	**CO3**
5.	Write an assembly code subroutine to approximate the square root of an argument using the bisection method.	**CO3**
6.	Write the Thumb code to multiply the two 32-bit in memory at addresses 0x1234_5678 and 0x7894_5612, storing the result in address 0x2000_0010.	**CO2**
7.	Write and compile assembly code and debug the program image on a MBED board (namely the Freedom KL25Z board) using the Keil MDK-ARM tool.	**CO4**
8.	Write a program to configure a General-Purpose Input Output (GPIO) peripheral in a low-level (register-level) in practice.	**CO3**
9.	Write and compile assembly code of I/O interfacing and debug the program image on a KL25Z board using the Keil MDKARM tool. Interface LEDs and Switches.	**CO5**
10.	Write and compile assembly code of Sensor interfacing and debug the program image on an KL25Z board using the Keil MDK-ARM tool. Interface PIR sensor-and DHT sensor.	**CO5**

Total Hours: 15 hrs.

Course Code: BECVL0512P	LAB Course Name: Thin Film Transistor Lab	L	T	P	C
Course Offered in: B. Tech. EE (VLSI)		0	0	2	1

Pre-requisite: Basics of Digital Electronics, VLSI Design Flow

Course Objectives:

Understand TFT device structures, materials, fabrication processes, and TCAD simulation techniques. Analyze TFT electrical characteristics and transport phenomena using simulation tools. To know reliability challenges and non-ideal effects in TFT devices. Design and simulate TFT-based analog and digital circuits for modern electronic applications. Apply TFT technologies to advanced display, 3D integration, and neuromorphic systems.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	TFT structures, materials, fabrication techniques, and TCAD simulation methodologies.	K3
CO2	Simulate and analyze TFT electrical characteristics and transport mechanisms using Silvaco tools.	K3
CO3	Evaluate non-ideal effects and reliability degradation in TFT devices.	K4
CO4	Design and simulate TFT-based digital and analog circuits for display and flexible electronics applications.	K4
CO5	Apply TFT technologies in advanced applications such as AMOLED displays, monolithic 3D integration, and neuromorphic systems.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	-	3	-	-	-	-	-	2	2	2	2
CO2	2	2	2	-	3	-	-	-	-	-	2	2	2	2
CO3	2	2	2	-	3	-	-	-	-	-	2	2	2	2
CO4	2	2	2	-	3	-	-	-	-	-	2	2	2	2
CO5	2	2	2	-	3	-	-	-	-	-	2	2	2	2

List Of Practical's (Indicative & Not Limited To)		**CO**
1.	Introduction to Silvaco TCAD Deck Build and Tony Plot environment	**CO1**
2.	Design of Bottom-Gate a- Si:H TFT structure using Silvaco	**CO1**
3.	Simulation of Poly-Si TFT fabrication process with crystallization techniques	**CO1**
4.	Simulation of IGZO TFT transfer and output characteristics	**CO2**
5.	Extraction of threshold voltage, mobility, and subthreshold swing parameters	**CO2**
6.	Energy band diagram and work function analysis of TFT structures	**CO2**
7.	Modeling of Density of States (DOS) and trap-assisted transport	**CO3**
8.	Analysis of Short Channel Effects and DIBL in TFT devices	**CO3**
9.	Simulation of kink effects in Poly-Si TFTs	**CO4**
10.	Reliability analysis under NBTI/PBTI and hot carrier stress conditions	**CO4**
11.	Design and simulation of TFT inverter and pseudo-CMOS logic circuits	**CO5**
12.	AMOLED pixel circuit simulation and monolithic 3D TFT application study	**CO5**

Total Hours: 15 hrs.

Course Code: BECVL0555	Course Name: System Verilog (Workshop-III)	L	T	P	C
Course Offered in: B. Tech ECE/ EE (VLSI)		0	0	6	3

Pre-requisite: Verilog HDL, Scripting.

Course Objectives:

The course aims to provide a comprehensive understanding of SystemVerilog for digital design and functional verification. It enables students to develop reusable verification environments using object-oriented programming, constrained-random testing, functional coverage, assertions, and Universal Verification Methodology (UVM) for protocol and system-level verification.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Describe SystemVerilog language fundamentals, data types, procedural blocks, and connectivity constructs used in digital design and verification.	K2
CO2	Apply object-oriented programming concepts for developing reusable and scalable verification components and testbenches.	K3
CO3	Develop verification infrastructures using constrained random verification, synchronization techniques, and functional coverage methodologies.	K4
CO4	Analyze and implement advanced verification techniques including assertions, thread control, and DPI-based interfacing.	K3
CO5	Design and verify protocol-based systems using UVM methodology and System Verilog-based verification environments.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	-	3	-	-	-	-	-	2	2	3	2
CO2	2	2	2	-	3	-	-	-	-	-	2	2	3	2
CO3	2	2	2	-	3	-	-	-	-	-	2	2	3	2
CO4	2	2	2	-	3	-	-	-	-	-	2	2	3	2
CO5	2	2	2	-	3	-	-	-	-	-	2	2	3	2

Course Contents / Syllabus

Unit 1	**System Verilog Language Fundamentals & Design Constructs**	**09 hours**

Data Types: 2-state vs. 4-state types, structures, unions, and enumerated types, Arrays & Queues: Packed and unpacked arrays, dynamic arrays, associative arrays, and queues, Procedural Blocks & Operators: Advanced operators, streaming operators, Tasks & Functions: Automatic and static functions, passing arguments, and void functions, Hierarchy & Connectivity: Packages, interfaces, mod ports, and clocking blocks

Unit 2	**Object-Oriented Programming (OOP) for Verification**	**09 hours**

Classes & Objects: Class properties, methods, constructors, and handles, Encapsulation & Inheritance: Data hiding, local/protected keywords, and class extension, Polymorphism & Abstraction: Virtual classes, virtual methods, and dynamic casting, OOP Applications: Layered testbenches, transaction-level modeling (TLM), and scoreboards

Unit 3	**Verification Infrastructure & Stimulus**	**09 hours**

Testbench Architecture: Generators, drivers, monitors, and reference models, Inter-process Synchronization: Semaphores, mailboxes, and events, Constrained Random Verification (CRV): inline constraints, solve-before constraints, and distribution, Functional Coverage: Cover groups, cover points, bins, cross coverage, and coverage system tasks

Unit 4	**Advanced Verification Concepts**	**09 hours**
System Verilog Assertions (SVA): Immediate and concurrent assertions, Sequences, properties, implication operators, and disable iff, Direct Programming Interface (DPI): Interfacing System Verilog with C/C++		
Unit 5	**Standard Verification Methodologies**	**09 hours**
Universal Verification Methodology (UVM): Introduction and architecture, Role of System Verilog classes in UVM-based verification Development of reusable verification environments, Hands-on testbench development and debugging techniques		
	Total Lecture Hours	**45 hours**

Textbook:

	Authors Name
1. System Verilog for Verification: A Guide to Learning the Testbench Language Features, Springer Publication, 2015.,	Chris Spear and Greg Tumbush
2. Writing Testbenches Using System Verilog, Springer Science & Business Media, 2006,	Janick Bergeron

Reference Books:

	Authors Name
1. System Verilog Assertions and Functional Coverage, Springer Publication, 2014.	Ashok B. Mehta

Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	https://youtu.be/YLczBemZpaE?si=wJCdoUed7epj52H9 https://youtu.be/Ke18NI5neoM?si=9XBokReDBnz_XAUg https://youtu.be/3g9cZFm-6J8?si=wZbWfGYeGqxtaz4R https://youtu.be/NpNw7yVmHck?si=0sUkrjedFXsHr0F4 https://youtu.be/m86zSu8vbZE?si=k33SXWofJUuf74Oc https://youtu.be/NpNw7yVmHck?si=0sUkrjedFXsHr0F4	00Hrs 25Min 01Hrs 51Min 03Hrs 48Min 10Hrs 18Min 01Hrs 20Min 01Hrs 15Min
Web References		

List of Practical

S. No.	**Name of Experiments/ Programs**	**CO**
1	Implementation and Simulation of Basic System-Verilog Data Types	**CO1**
2	Implementation of Packed and Unpacked Arrays	**CO1**
3	Implementation of Dynamic Arrays and Queues	**CO2**
4	Implementation of Tasks and Functions	**CO2**
5	Implementation of Packages and Modular Design	**CO3**
6	Implementation of Classes and Objects	**CO3**
7	Implementation of Inheritance and Polymorphism	**CO4**
8	Verification Using Mailbox, Events and Constrained Randomization	**CO4**
9	Functional Coverage Using Cover-groups and Cover-points	**CO5**
10	Implementation of System-Verilog Assertions (SVA)	**CO5**
		Total Hours: 35 hrs.

Course Code: BECVL0601	Course Name: Low Power VLSI Design	L	T	P	C
Course Offered in: B.Tech. EE (VLSI)		3	1	0	4

Pre-requisite: Basic knowledge of Digital Electronics, CMOS circuits, MOSFET operation, and VLSI Design fundamentals.

Course Objectives:

This course provides an understanding of power dissipation in digital integrated circuits and introduces low-power VLSI design techniques for energy-efficient system design. It covers the design and analysis of low-power, high-speed arithmetic circuits such as adders and multipliers, along with low-voltage memory architectures. The course enables students to evaluate and apply power optimization strategies while maintaining system performance and reliability.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Demonstrate the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.	K3
CO2	Illustrate the different low-power design approaches and optimization of switched capacitance.	K3
CO3	Discuss the different low-power high speed adders.	K2
CO4	Apply the concepts of low voltage and low power to different multipliers.	K3
CO5	Apply the concepts of low voltage and low power to different memories.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	-	-	-	-	-	-	-	-	2	3	2
CO2	3	2	2	-	-	-	-	-	-	-	-	2	3	2
CO3	3	2	2	-	-	-	-	-	-	-	-	2	3	2
CO4	3	2	2	-	-	-	-	-	-	-	-	2	3	2
CO5	3	2	2	-	-	-	-	-	-	-	-	2	3	2

Course Contents / Syllabus

Unit 1	**Fundamentals of Low Power VLSI Design**	**09 hours**

Need for Low Power Circuit Design, Sources of Power Dissipation — Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation-Reverse diode leakage current, Sub threshold leakage current, Glitching Power Dissipation.

Unit 2	**Low Voltage Process Technology**	**09 hours**

Low-Power Design through Voltage Scaling: VTCMOS circuits, MTCMOS circuits, Architectural Level Approach — Pipelining and Parallel Processing Approaches. Estimation and Optimization of Switching Activity: The Concept of Switching Activity, Reduction of Switching Activity, Reduction of Switched Capacitance-System Level Measures, Circuit Level Measures, and Mask level Measures.

Unit 3	**Low-Voltage Low-Power Adders**	**09 hours**

Introduction, Standard Adder Cells, CMOS Adder's Architectures — Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Carry Skip Adders.

Unit 4	**Low-Voltage Low-Power Multipliers**	**09 hours**

Overview of Multiplication, Booth Multiplier-Booth's algorithm, modified Booth algorithm, Introduction to Tree Multiplier (Wallace and Dada multipliers) and 4:2 Compressors.

Unit 5	**Low Power Random Access Memory Circuits**	**09 hours**

Sources of power dissipation in SRAMs, Low power SRAM circuit techniques, Sources of power dissipation in DRAMs, Low power DRAM circuit techniques.		
	Total Lecture Hours	**45 hours**
Textbook:		
	Authors Name	
1.CMOS Digital Integrated Circuits — Analysis and Design, TMH, 2011,	Sung-Mo Kang, Yusuf Leblebici	
2.Low-Voltage, Low-Power VLSI Subsystems, TMH Professional Engineering., 7th Edition, 2004,	Kiat-Seng Yeo, Kaushik Roy	
Reference Books:		
	Authors Name	
1. Principles of CMOS VLSI Design, 2nd Edition, Addison Wesley (Indian reprint),	Neil H. E. Weste and K. Eshraghian.	
2. Low Power VLSI CMOS Circuit Design, Kluwer Academic Press, 1995,	Bellamour, and M. I. Elmasri.	
3. Low Power Digital CMOS Design, Kluwer Academic Publishers, 1995,	Anantha P. Chandrakasan and Robert W. Brodersen.	
4. Low-Power CMOS VLSI Design, Wiley-Interscience, 2000.	Kaushik Roy and Sharat C. Prasad	
Self-Study Content Links:		Duration (in Hrs)
MOOCs		
Video Lectures	https://www.youtube.com/watch?v=C8kiblD2riw&list=PL1wj50dotxPPsCrF16rHnkfID1TP2LJ5Z	00Hrs 25Min
	https://www.youtube.com/watch?v=0ykJeTGqv6M&list=PLB3F0FC99B5D89571&index=27	01Hrs 51Min
	https://www.youtube.com/watch?v=K2kL7pMnL_0&list=PLVDb88QIgXkeeUo6I2oudLvc76GbLGrTi	03Hrs 48Min
	https://www.youtube.com/watch?v=ORtlxpW_LMU&t=10s	10Hrs 17Min
	https://www.youtube.com/watch?v=EMcW9EggY0s	01Hrs 25Min
	https://www.youtube.com/watch?v=jK6xr4r06tU&list=PLB3F0FC99B5D89571&index=16	00Hrs 55Min
Web References		

Course Code: BECVL0602	Course Name: VLSI Testing and Testability	L	T	P	C
Course Offered in: B.Tech. ECE/ EE (VLSI)		3	1	0	4

Pre-requisite: Fundamental knowledge of VLSI circuits.

Course Objectives:

The course aims to provide a comprehensive understanding of testing and design-for-testability (DFT) techniques for integrated circuits to enhance design quality and manufacturing yield. It enables students to analyze test generation methods for combinational and sequential circuits, implement memory testing and Built-In Self-Test (BIST) techniques, and understand UVM-based verification environments for modern VLSI design verification.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Apply the concepts in testing which can help them design a better yield in IC design	K3
CO2	Analyze the various test generation methods for combinational circuits	K4
CO3	Analyze the various test generation methods for sequential circuits.	K4
CO4	Identify the design for testability methods for different memory circuits	K2
CO5	Recognize BIST techniques for enhancing testability and explain the hierarchy and structure of UVM-based verification environments.	K2

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	-	-	-	-	-	-	-	-	2	3	2
CO2	2	2	2	-	-	-	-	-	-	-	-	2	3	2
CO3	2	2	2	-	-	-	-	-	-	-	-	2	3	2
CO4	2	2	2	-	-	-	-	-	-	-	-	2	3	2
CO5	2	2	2	-	-	-	-	-	-	-	-	2	3	2

Course Contents / Syllabus

Unit 1	**Introduction to VLSI Testing and Fault Modelling**	**09 hours**

Importance and Principle of testing, Challenges in VLSI testing, Levels of abstractions in VLSI testing, Functional vs. Structural approach to testing, Complexity of the testing problem, Types of Testing, DC and AC parametric tests Fault Modelling: Stuck at fault, fault equivalence, fault collapsing, fault dominance, fault simulation

Unit 2	**Testing And Testability of Combinational Circuits**	**09 hours**

Test Generation Basics: Test generation algorithms, Random test generation, ATPG algorithms for combinational circuits, Boolean difference, Path sensitization, D – algorithm, PODEM, Testable combinational logic circuit design

Unit 3	**Testing And Testability of Sequential Circuits**	**09 hours**

Testing of sequential circuits as iterative combinational circuits, state table verification, test generation based on circuit structure, Sequential ATPG, Ad Hoc design rules, Level Sensitive Scan Design, Scan path technique (scan design), partial scan, Boundary scan

Unit 4	**Memory, Delay, Fault and IDDQ Testing**	**09 hours**

Testable memory design, RAM fault models, Test algorithms for RAM, Delay faults, Delay tests, IDDQ testing, Testing methods, Limitations of IDDQ testing.

Unit 5	**Built In Self-Test (Bist) Techniques**	**09 hours**

Built-in self-test (BIST): Design rules, Exhaustive testing, Pseudo-random testing, Pseudo-exhaustive testing, Output response analysis, Logic BIST architectures, Introduction to Test compression, Introduction to Universal Verification Methodology (UVM), Hierarchy in UVM

		Total Lecture Hours | **45 hours**
Textbook:		
	Authors Name	
1.An Introduction to Logic Circuit Testing,	Morgan & Claypool Publishers, Parag K. Lala	
2.Essentials of Electronic Testing for Digital, Memory and Mixed Signal VLSI Circuits, Kluwar Academic Publishers,2000.	M. L. Bushnell and V. D. Agrawal.	
3.Digital System Testing and Testable Design, Jaico Publishing House,	M. Abramovici, M.Breuer, and A. Friedman.	
Reference Books:		
	Authors Name	
1. Introduction to Formal Hardware Verification, Springer.	Thomas Kropf.	
2. Digital Systems and Testable Design, Jaico Publishing House.	M. Abramovici, M.A. Breuer and A.D. Friedman.	
3. VLSI Test Principles and Architectures Design for Testability, Morgan Kaufmann Publishers, 2006.	W.W. Wen	
4. Design Test for Digital IC's and Embedded Core Systems, Prentice Hall International.	A.L. Crouch.	
Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	1.https://www.youtube.com/watch?v=ynKZLc-wtQA	00Hrs 25Min
	2. https://youtu.be/ottMYN7yg8s?si=kMXFQhyfsIjZo3Ip	01Hrs 51Min
	3. https://www.youtube.com/watch?v=MgCFUO2BrkQ	03Hrs 48Min
	4. https://youtu.be/ottMYN7yg8s?si=Ki5KgxPZswrNsZPV	10Hrs 17Min
	5. https://youtu.be/hXYAc8L2pR8?si=NmglQNWr0j3CvLUH	00Hrs 28Min
	6. https://www.youtube.com/watch?v=X7oB78Rq-0s	00Hrs 35Min
	7. https://youtu.be/FQM1PstP-9o?si=amTsmmwEhQYvJ9Rl	01Hrs 50Min
	8. https://youtu.be/DPKRRhHrYmA?si=YOZ6byTc1I_W6SZI	01Hrs 25Min
	9. https://youtu.be/y9LSEWmtkKg?si=10ai7oaY6EkkKHX_	01Hrs 31Min
	10. https://youtu.be/-fHPExqz8TQ?si=I4-G9Mp-rWf2t5gG	00Hrs 45Min
	11. https://www.youtube.com/watch?v=xAhbTylDT6k	02Hrs 50Min
	12. https://youtu.be/fbl1ykBW53U?si=6sWIM1r4Kr4YKt3A	01Hrs 25Min
	13. https://youtu.be/USxZIVRZ2xA?si=fTKxqxIWmUqHm7td	02Hrs 31Min
Web References		

Course Code: BEC0612	Course Name: Image Processing and Pattern Recognition	L	T	P	C
Course Offered in: B.Tech. ECE / EE (VLSI		3	0	0	3

Pre-requisite: Basic knowledge of mathematics (linear algebra, probability) and fundamental programming concepts (e.g., MATLAB/Python).

Course Objectives:

This course introduces the fundamental concepts of digital image processing, including image representation, enhancement, restoration, and segmentation techniques. It enables students to apply spatial and frequency domain methods, noise reduction approaches, and analytical tools for image analysis, feature extraction, and interpretation of visual information.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Describe the fundamental concepts of digital image processing and image formation.	K2
CO2	Apply image enhancement techniques in spatial and frequency domains.	K3
CO3	Recognize various noises in images and apply restoration methods	K2
CO4	Apply different segmentation techniques on image.	K3
CO5	Apply knowledge of mathematics for image understanding and analysis.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	-	-	-	-	-	-	-	-	2	2	3
CO2	3	2	2	-	-	-	-	-	-	-	-	2	2	3
CO3	3	2	2	-	-	-	-	-	-	-	-	2	2	3
CO4	3	2	2	-	-	-	-	-	-	-	-	2	2	3
CO5	3	2	2	-	-	-	-	-	-	-	-	2	2	3

Course Contents / Syllabus

Unit 1	**Digital Image Processing**	**09 hours**

Digital Image Processing: Definition, Basic image file formats, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Image Sensing and Acquisition, Image Sampling and Quantization, Basic Relationship between Pixels, Applications of DIP.

Unit 2	**Image Enhancement**	**09 hours**

Spatial Domain: Basic Gray Level Transformations, Histogram based Processing, Enhancement using Arithmetic/Logic Operations, Spatial Filtering: Smoothing and Sharpening Filter. Frequency Domain: Image Smoothing and Image Sharpening Using Frequency Domain Filters, Homomorphic Filtering.

Unit 3	**Image Restoration**	**09 hours**

Image Degradation/Restoration process model, Noise Models, Restoration in the presence of noise only spatial filtering, Periodic noise reduction by frequency domain filtering. Compression: Lossless compression: Variable length coding, LZW coding, Bit plane coding, Predictive coding-DPCM, Lossy Compression: Transform coding, Wavelet coding, Basics of Image compression standards: JPEG, MPEG, HEIF/HEIC and WebP.

Unit 4	**Image Segmentation and Image/Object Feature Extraction**	**09 hours**

Line and Edge Detection, Thresholding: Otsu and Adaptive, Region-Based Segmentation, Morphological Watershed, K-means and Fuzzy C-means, Wavelet Transform, Discrete Wavelet Transform, Hough Transform.

Unit 5	**Color Image Processing & Morphological Filtering Basis**	**09 hours**

Fundamentals of different color models - RGB, CMY, HSI, YCbCr, Lab; False color; Pseudo color; Enhancement; Segmentation, Dilation and Erosion Operators, Top Hat Filters.		
	Total Lecture Hours	**45 hours**
Textbook:		
	Authors Name	
1.Digital Image Processing Pearson, Third Edition, 2010.	Rafael C. Gonzalez.	
2."Fundamentals of Digital Image Processing Pearson, 2002.	Anil K. Jain.	
Reference Books:		
	Authors Name	
1. Image Processing, Analysis and Machine Vision, 2nd ed., Thomson Learning, 2001;	Milan Sonka, Vaclav Hlavav, Roger Boyle.	
2. Digital Image Processing, 3rd Edition;	Rafael C Gonzalez and Richard E Woods.	
3. Digital Image Processing‖, 3rd ed., John Wiley & Sons, 2007;	Pratt W. K.	
Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	https://youtube.com/playlist?list=PL1F076D1A98071E24&si=2cIpmH8Tgpjldqtr https://youtube.com/playlist?list=PL1F076D1A98071E24&si=2cIpmH8Tgpjldqtr https://youtube.com/playlist?list=PL1F076D1A98071E24&si=2cIpmH8Tgpjldqtr https://youtube.com/playlist?list=PL1F076D1A98071E24&si=2cIpmH8Tgpjldqtr https://youtube.com/playlist?list=PL1F076D1A98071E24&si=2cIpmH8Tgpjldqtr	00Hrs 25Min 01Hrs 51Min 03Hrs 48Min 10Hrs 17Min 01Hrs 22Min
Web References		

Course Code: BEC0617	Course Name: Big Data Analytics for IoT and Internet of Everything	L	T	P	C
Course Offered in: B.Tech. ECE/VLSI		**3**	**0**	**0**	**3**

Pre-requisite: Basic Knowledge of IoT and IoT Protocols

Course Objectives:

The course aims to develop problem-solving and programming skills by enabling students to analyze computational problems, design algorithms, and implement solutions using appropriate programming constructs and data representations. It also builds a strong programming foundation, preparing students to adapt easily to other programming languages and software development environments.

Course Outcome: After completion of the course, the student will be able to		**Blooms' Level**
CO1	Identify the concept of big data platforms for IoT.	K2
CO2	Analyze the concept of Sustainability Data and Analytics in Cloud-Based M2M Systems.	K4
CO3	Explain the YARN and HDFS in Data management.	K2
CO4	Analyze Map Reduce framework and demonstrate its use in features extraction.	K4
CO5	Describe the various types of Google and AWS data analytics tools.	K2

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	-	-	-	-	-	-	-	-	2	2	3
CO2	2	2	2	-	-	-	-	-	-	-	-	2	2	3
CO3	2	2	2	-	-	-	-	-	-	-	-	2	2	3
CO4	2	2	2	-	-	-	-	-	-	-	-	2	2	3
CO5	2	2	2	-	-	-	-	-	-	-	-	2	2	3

Course Contents / Syllabus

Unit 1	**Big data platforms for the internet of Things**	**09 hours**

Big Data Platforms for the Internet of Things: network protocol, data dissemination, current state of art improving Data and Service Interoperability with Structure, Compliance, Conformance and Context Awareness, interoperability problem in the IoT context, Big Data Management Systems for the Exploitation of Pervasive Environments, Big Data challenges and its requirements, Types of data.

Unit 2	**Sustainability Data and Analytics**	**09 hours**

Sustainability Data and Analytics: Sustainability Data and Analytics in Cloud-Based M2M Systems, Potential stakeholders and their complex relationships to data and analytics applications, Social Networking Analysis, building a useful understanding of a social network, leveraging social media and IoT to Bootstrap Smart Environments, Lightweight Cyber Physical Social Systems, Citizen actuation.

Unit 3	**Hadoop Architecture**	**09 hours**

Hadoop Eco System and YARN: Hadoop ecosystem components, schedulers, fair and capacity, Hadoop 3.x, New Features — Name Node high availability, HDFS federation, MRv2, YARN, Running MRv1 in YARN. HDFS (Hadoop Distributed File System): Design of HDFS, HDFS concepts, benefits and challenges, file sizes, block sizes and block abstraction in HDFS, data replication, how does HDFS store, read, and write files, Java Interfaces to HDFS, command-line interface, Hadoop file system interfaces, data flow, data ingest with Flume and Scoop, Hadoop archives, Hadoop I/O: compression, serialization, Avro and file-based data structures.

Unit 4	Hadoop and Map Reduce	09 hours
Hadoop: History of Hadoop, Apache Hadoop, the Hadoop Distributed File System, components of Hadoop, data format, analyzing data with Hadoop, scaling out, Hadoop streaming, Hadoop pipes, Hadoop Echo System. Map Reduce: Map Reduce framework and basics, how Map Reduce works, developing a Map Reduce application, unit tests with MR unit, test data and local tests, anatomy of a Map Reduce job run, failures, job scheduling, shuffle and sort, task execution, Map Reduce types, input formats, output formats, Map Reduce features, Real-world Map Reduce.		
Unit 5	**Google and AWS Data Analytics Tools**	**09 hours**
Google Data Analytics Tools: Google Analytics, Google Search Console, Looker, Google Ads, Google Data Studio, Google Optimize, Google Surveys, Google Tag Manager, Google Big Query. AWS Data Analytics Tools: Amazon Athena, Amazon EMR, Amazon Redshift, Amazon Kinesis, Amazon OpenSearch Service, Amazon QuickSight, AWS Glue Data Brew.		
	Total Lecture Hours	**45 hours**

Textbook:	
	Authors Name
1.Big Data, Big Analytics: Emerging Business Intelligence and Analytic Trends for Today's Businesses Wiley, 2013.	Michael Minelli, Michelle Chambers, and Ambiga Dhiraj
2. Big-Data Black Book, DT Editorial Services, Wiley India.	DT Editorial Services
3.Hadoop: The Definitive Guide, Third Edition, O'Reilly, 2012.	Tom White.
4. Hadoop Operations, O'Reilly, 2012.	Eric Sammer.

Reference Books:	
	Authors Name
1.Big Data and The Internet of Things Enterprise Information Architecture for A New Age, Apress, 2015.	Stackowiak R, Licht A, Mantha V, Nagode L
2.Thingalytics - Smart Big Data Analytics for the Internet of Things, 2015.	Dr. John Bates

Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	1. https://www.youtube.com/live/e3D0gNqfnzo?feature=share 2. https://youtu.be/CDgtvl4c9Pg 3. https://youtu.be/FispS3Jx_3g 4. https://www.youtube.com/watch?v=mNP44rZYiAU 5. https://youtu.be/K-FhMegdlJo	01Hrs 05Min 00Hrs 25Min 01Hrs 15Min 03Hrs 48Min 10Hrs 17Min
Web References		

Course Code: BECVL0611	Course Name: OLED & QLED	L	T	P	C
Course Offered in: B.Tech. ECE / VLSI		3	0	0	3

Pre-requisite: Basic undergraduate-level knowledge of Semiconductors, Optics, Electronics and Quantum Mechanics.

Course Objectives:

This course introduces the fundamentals of OLED and QLED display technologies, including their device physics, materials, and fabrication processes. It covers VLSI-based pixel circuit design, performance evaluation, reliability considerations, and emerging display technologies for next-generation electronic displays.

Course Outcome: After completion of the course, the student will be able to		**Blooms' Level**
CO1	Explain OLED and QLED working principles	K2
CO2	Analyze materials and device structures.	K3
CO3	Design pixel driving circuits using VLSI concepts.	K3
CO4	Evaluate performance and reliability metrics.	K3
CO5	Interpret emerging display technologies.	K4

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	-	-	-	-	-	-	-	-	2	2	2
CO2	2	2	2	-	-	-	-	-	-	-	-	2	2	2
CO3	2	2	2	-	-	-	-	-	-	-	-	2	2	2
CO4	2	2	2	-	-	-	-	-	-	-	-	2	2	2
CO5	2	2	2	-	-	-	-	-	-	-	-	2	2	2

Course Contents / Syllabus

Unit 1	**Fundamentals of Display Technologies**	**09 hours**

Evolution: CRT, LCD, LED, OLED, QLED, Emissive vs non-emissive displays, Basic photometric concepts: luminance, brightness, contrast ratio Color science: CIE diagram, color gamut, Human visual perception.

Unit 2	**OLED Technology – Devices and Materials**	**09 hours**

Organic semiconductor fundamentals, Working principle of OLED, Charge injection, transport, recombination
OLED structures: PMOLED and AMOLED Materials: Anode (ITO), cathode metals, HTL, ETL, emissive layer
Efficiency metrics: IQE, EQE Degradation mechanisms and lifetime issues

Unit 3	**OLED Fabrication and Driving Circuits**	**09 hours**

OLED device structure and layer engineering, Fabrication techniques: Vacuum thermal evaporation (VTE), Inkjet printing Encapsulation methods, AMOLED pixel circuits: 2T1C, 5T1C, 7T1C, Threshold voltage compensation techniques, CMOS backplane technologies (LTPS, IGZO), Power consumption optimization

Unit 4	**QLED Technology – Fundamentals and Devices**	**09 hours**

Introduction to Quantum Dots (QDs), Quantum confinement effect, Optical properties and size-dependent emission
QLED types: Photoluminescent QLED (QDEF), Electroluminescent QLED Device structure: ETL, QD layer, HTL Materials: CdSe, InP-based QDs Charge transport and recombination in QLEDs.

Unit 5	**QLED Circuits, Comparison and Advanced Trends**	**09 hours**

QLED pixel architecture and driving methods, Comparison with OLED: Efficiency, Lifetime, Color purity, Power consumption Reliability issues: OLED burn-in, QLED stability, Flexible and transparent displays, Micro-LED vs OLED vs QLED, Applications in AR/VR, IoT, wearable electronics.

	Total Lecture Hours	**45 hours**

Textbook:		
		Authors Name
1. OLED Display Fundamentals and Applications, Wiley, 2nd Edition, 2017.		Takatoshi Tsujimura.
2. Organic Light Emitting Devices: Synthesis, Properties and Applications, Wiley-VCH, 2006.		Klaus Müllen and Ullrich Scherf (Eds.)
3. Organic Light-Emitting Devices: A Survey, Springer, 2004.		Joseph Shinar (Ed.)
Reference Books:		
		Authors Name
1. Fabrication Engineering at the Micro and Nanoscale, Oxford University Press, 3rd Edition, 2012.		Stephen A. Campbell
2. Solid State Electronic Devices, Pearson, 7th Edition, 2015.		Ben G. Streetman and Sanjay Kumar Banerjee
Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	1.https://youtu.be/CoBIpAZQYiA?si=K0ucKGL3PU7gIDlE 2. https://youtu.be/d1Lk7EL-XEo?si=vb3zxyVZoBW5VVnr	01Hrs 51Min 03Hrs 48Min
Web References		

Course Code: BEC0615	Course Name: ANN & Deep Learning	L	T	P	C
Course Offered in: B.Tech. ECE / VLSI		3	0	0	3

Pre-requisite: Working knowledge of Linear Algebra, Probability Theory. It would be beneficial if the participants have done a course on Machine Learning.

Course Objectives:

Given a computational problem, identify and abstract the programming task involved. Approach the programming tasks using techniques learned and writepseudo-code. Choosethe right data representation formats based on the requirements of the problem. Use comparisons and limitations of the various programming constructs and choose the right one for the task in hand. By learning the basic programming constructs, students can easily switch over to any other language in future.

Course Outcome: After completion of the course, the student will be able to		**Blooms' Level**
CO1	Describe the fundamental concepts, history, and architecture of neural networks and deep learning.	K2
CO2	Implement and analyze gradient-based optimization algorithms and dimensionality reduction techniques like PCA.	K3
CO3	Apply regularization methods and optimization strategies to train efficient deep learning models.	K3
CO4	Compare and contrast popular deep learning architectures such as CNNs (LeNet, AlexNet, VGG, ResNet, etc.).	K2
CO5	Design and implement RNN, LSTM, and GRU-based models for sequential data analysis.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	-	-	-	-	-	-	-	2	2	2	3
CO2	3	3	2	-	-	-	-	-	-	-	2	2	2	3
CO3	3	3	2	-	-	-	-	-	-	-	2	2	2	3
CO4	3	3	2	-	-	-	-	-	-	-	2	2	2	3
CO5	3	3	2	-	-	-	-	-	-	-	2	2	2	3

Course Contents / Syllabus

Unit 1	**Introduction**	**09 hours**

Introduction: History of Deep Learning, Deep Learning Success Stories, McCulloch Pitts Neuron, ANN and its types, Multilayer Perceptron's (MLPs), Representation Power of MLPs, Sigmoid Neurons, RELU activation, Gradient Descent, Activation Functions, Loss Functions, Feed Forward Neural Networks, Back propagation.

Unit 2	**Optimization & Dimensionality Reduction**	**09 hours**

Gradient Descent (GD), Momentum Based GD, Nesterov Accelerated GD, Stochastic GD, Principal Component Analysis and its interpretations, Singular Value Decomposition, Auto encoders and relation to PCA, Regularization in auto encoders, De-noising auto encoders, Sparse auto encoders.

Unit 3	**Deep Learning Fundamentals**	**09 hours**

Regularization: Bias Variance Trade-off, L1 and L2 regularization, Drop-outs, Early stopping, Dataset augmentation, Greedy Layer-wise Pretraining, Soft-max layer, Weight initialization methods, Batch Normalization, Learning Vectorial Representations of Words.

Unit 4	**Deep learning architectures**	**09 hours**

Convolutional Neural Networks: Convolution, Padding, Stride, Pooling, LeNet, AlexNet, ZF-Net, VGGNet, ResNet, DenseNet.

Unit 5	RNN and LSTM models	09 hours
Recurrent Neural Networks, Back propagation through time (BPTT), Vanishing and Exploding Gradients, Truncated BPTT, GRU, LSTMs, Encoder Decoder Models.		
	Total Lecture Hours	**45 hours**
Textbook:		
		Authors Name
1. "Deep learning", MIT Press, 2016;		Ian Goodfellow and Yoshua Bengio and Aaron Courville
2. "Artificial neural network" PHI Publication.;		B. Yegnanarayana
Reference Books:		
		Authors Name
1. "Neural Networks and Deep Learning", Determination Press, 2015;		Nielsen, Michael A.
2. "Machine Intelligence: Demystifying Machine Learning, Neural Networks and Deep Learning", Notion Press, 2019.;		Suresh Samudrala.
3. "Neural Networks", Tata Mc Graw Hill.,		Kumar Satish.
Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	https://www.youtube.com/playlist?list=PLEAYkSg4uSQ1r-2XrJ_GBzzS6I-f8yfRU	10Hrs 25Min
	https://www.youtube.com/watch?v=QK7GJZ94qPw	01Hrs 51Min
	https://www.youtube.com/playlist?list=PLEAYkSg4uSQ1r-2XrJ_GBzzS6I-f8yfRU	02Hrs 48Min
	https://www.youtube.com/watch?v=IHZwWFHWa-w	10Hrs 17Min
	https://www.youtube.com/playlist?list=PLEAYkSg4uSQ1r-2XrJ_GBzzS6I-f8yfRU	00Hrs 25Min
	https://www.youtube.com/playlist?list=PLVHz9YUo4rRd5ZmGg8Kq0S1tIi7hthm4V	01Hrs 22Min
	https://www.youtube.com/playlist?list=PLEAYkSg4uSQ1r-2XrJ_GBzzS6I-f8yfRU	03Hrs 48Min
	https://www.youtube.com/playlist?list=PLVHz9YUo4rRd5ZmGg8Kq0S1tIi7hthm4V	10Hrs 17Min
	https://www.youtube.com/watch?v=AsNTP8Kwu80	01Hrs 11Min
	https://www.youtube.com/playlist?list=PLEAYkSg4uSQ1r-2XrJ_GBzzS6I-f8yfRU	01Hrs 34Min
Web References		

Course Code: BEC0616	Course Name: Real Time Operating System	L	T	P	C
Course Offered in: B. Tech ECE		3	0	0	3

Pre-requisite: Basic fundamental of microprocessor, microcontroller & Embedded System

Course Objectives:

This course develops problem-solving skills through programming by enabling students to analyze computational problems, design algorithms, and write effective pseudocode. It emphasizes the selection of appropriate data representations and programming constructs while building a strong foundation that facilitates learning advanced programming languages and real-time operating system concepts.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Explain the basics Embedded Operating System internals.	K2
CO2	Describe the basic concepts of RTOS.	K2
CO3	Apply the concepts of Process and Task Scheduling.	K3
CO4	Implement strategies to interface memory and I/O with RTOS kernel.	K3
CO5	Analyze the architecture of CMSIS-RTOS & process of RTX task management.	K4

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	-	-	-	-	-	-	-	-	2	2	3
CO2	2	2	2	-	-	-	-	-	-	-	-	2	2	3
CO3	2	2	2	-	-	-	-	-	-	-	-	2	2	3
CO4	2	2	2	-	-	-	-	-	-	-	-	2	2	3
CO5	2	2	2	-	-	-	-	-	-	-	-	2	2	3

Course Contents / Syllabus

Unit 1	**Linux Internals**	**09 hours**

Linux internals: Process Management, File Management, Memory Management, I/O Management. Overview of POSIX APIs, Threads – Creation, Cancellation, POSIX Threads Inter Process Communication – Semaphore, Pipes, FIFO, Shared Memory Kernel: Structure, Kernel Module Programming, Interfacing: Serial, Parallel Interrupt Handling Linux Device Drivers: Character, USB, Block & Network.

Unit 2	**OS Overview**	**09 hours**

OS overview: OS components, OS structure, Types of Operating Systems, Basics of RTOS: Real-time concepts, Characteristics of RTOS, Architecture of RTOS, Classification of RTOS: Hard Real time and Soft Real-time, Firm real time system, Advantage and disadvantage of RTOS.

Unit 3	**Process Management**	**09 hours**

Process: Introduction, Memory lay out of an executing program, Process types, Schedulers and Types of scheduling, Scheduling Process control block, Process creation, Process Termination, Context Switching and States.

Unit 4	**Concurrency & Memory Management**	**09 hours**

Concurrency: Concurrency Scheduling, Multiprocessing environment, Read-write by multiple CPUs and consistency problem, Solutions with Mutual Exclusion, Hardware Mutex, Software Mutex, Example: Dekker's algorithm, Semaphore, Deadlock, Banker's algorithm. Memory Management: Processes Need Memory, Address Binding & its types, Memory Hierarchy, Virtual Memory, Memory Partitioning, Paging, Segmentation with Paging, File System, File Structure, Directory Structure, Disk, Interrupt & DMA.

Unit 5	**Introduction to RTX**	**09 hours**
RTX: RTX structure, RTX files, RTX task and time management, Simple Time Management APIs, Task Priority Scheme in RTX, Inter-Task Communication, Event, Interrupt, Mutex, Semaphore, Mailboxes and Messages in RTX, RTX control functions, Architecture of CMSIS-RTOS.		
	Total Lecture Hours	**45 hours**

Textbook:	
	Authors Name
1. Real-Time Operating Systems for ARM Cortex-M Microcontrollers, 4th Edition.2017.	Jonathan W. Valvano.
2.Real-Time Concepts for Embedded Systems, CMP Books, Elsevier, 2003.	Qing Li and Carolyn Yao.
3. The Real-Time Kernel, CMP Books 2002.	Jean J. Labrosse.
Reference Books:	
	Authors Name
1. Embedded Systems: Architecture, Programming and Design, McGraw Hill, 2017.	Raj Kamal.
2. Building Embedded Linux Systems, O'Reilly Publications.2008.	Karim Yaghmour.

Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	1.https://nptel.ac.in/courses/106106144 2.https://nptel.ac.in/courses/106105159 3. https://nptel.ac.in/courses/106105159 4.https://onlinecourses.nptel.ac.in/e-learning/preview/noc25_cs78 5. https://www.youtube.com/watch?v=OrM7nZcxXZU 6. https://www.youtube.com/watch?v=eESIFJz7mJw 7. https://www.youtube.com/watch?v=Rtewg5tbjqY	00Hrs 25Min 01Hrs 51Min 03Hrs 48Min 10Hrs 17Min 00Hrs 25Min 01Hrs 30Min 01Hrs 45Min 00Hrs 53Min
Web References		

Course Code: BECVL0612	Course Name: Emerging Memory Devices	L	T	P	C
Course Offered in: B.Tech. ECE / VLSI		3	0	0	3

Pre-requisite: Basic undergraduate-level knowledge of Semiconductors.

Course Objectives:

This course introduces the fundamentals and operating principles of emerging memory technologies, including RRAM, PCM, MRAM, and ferroelectric memories. It covers their device characteristics, architectures, and applications, while exploring advanced memory concepts for neuromorphic computing, artificial intelligence, and high-performance in-memory computing systems.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Describe the fundamentals and classifications of emerging memory technologies.	K2
CO2	Analyze switching mechanisms and characteristics of RRAM and PCM devices.	K4
CO3	Evaluate MRAM and ferroelectric memory architectures and operational principles.	K5
CO4	Examine advanced memory technologies and neuromorphic devices.	K4
CO5	Analyze memory architectures and applications in AI and in-memory computing systems.	K4

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	-	-	-	-	-	-	-	-	2	3	2
CO2	2	2	2	-	-	-	-	-	-	-	-	2	3	2
CO3	2	2	2	-	-	-	-	-	-	-	-	2	3	2
CO4	2	2	2	-	-	-	-	-	-	-	-	2	3	2
CO5	2	2	2	-	-	-	-	-	-	-	-	2	3	2

Course Contents / Syllabus

Unit 1	**Introduction to Semiconductor Memory Technologies**	**09 hours**

Overview of Memory Hierarchy, Conventional Memories: SRAM, DRAM, EEPROM, Flash, Limitations of CMOS Scaling in Conventional Memories, Need for Emerging Non-Volatile Memories (NVMs), Performance Parameters: Speed, Power Consumption Retention, Endurance, Scalability, Classification of Emerging Memory Devices.

Unit 2	**Resistive and Phase Change Memory Devices**	**09 hours**

Resistive Random Access Memory (RRAM/ReRAM): Device Structure and Materials, Filamentary and Interface Switching, Mechanisms Bipolar and Unipolar Switching, Crossbar Array Architecture, Sneak Path Current Issues
Phase Change Memory (PCM/PRAM): Chalcogenide Materials, Amorphous and Crystalline States, SET and RESET Operations, Thermal Effects and Programming Techniques, Applications and Challenges

Unit 3	**Magnetic and Ferroelectric Memory Technologies**	**09 hours**

Magnetic Random Access Memory (MRAM)Spintronics Fundamentals, Magnetic Tunnel Junction (MTJ), STT-MRAM and SOT-MRAM, Switching Dynamics, Reliability and Energy Efficiency
Ferroelectric Memories: Ferroelectric Materials and Polarization, FeRAM Architecture and Operation, Ferroelectric Tunnel Junctions (FTJ), FeFET-based Memory Devices, Advantages and Scaling Challenges

Unit 4	**Advanced Emerging Memory Devices**	**09 hours**

Conductive Bridge RAM (CBRAM), Electrochemical RAM (ECRAM),2D Material-Based Memories, Racetrack Memory, Ultra RAM Memristor Fundamentals and Characteristics, Neuromorphic and Synaptic Memory Devices.

Unit 5	**Memory Architectures and Applications**	**09 hours**

Memory Array Design,1T1R and Cross-Point Architectures, Selector Devices, Reliability Issues: Variability, Retention, Endurance Thermal Stability, In-Memory Computing, AI Hardware Accelerators, Neuromorphic Computing Applications, Future Trends in Emerging Memory Technologies.		
Total Lecture Hours		**45 hours**
Textbook:		
		Authors Name
1. Semiconductor Memory Devices and Circuits, CRC Press.		S. Yu
2. Emerging Memory Technologies: Design, Architecture and Applications.		Yuan Xie
Reference Books:		
		Authors Name
1. Resistive Switching: From Fundamentals of Nanoionic Redox Processes to Memristive Device Applications.		D. Ielmini and H.-S. P. Wong
Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	https://youtu.be/CXFtbpYaBXw https://youtu.be/smKQtZUhtBQ https://youtu.be/iBGgzrvwFi8 https://youtu.be/dsqbiIW9tEc https://youtu.be/EElJ-oCgWEI https://youtu.be/iBGgzrvwFi8?si=yISnwWWyqQMYkV2w https://www.youtube.com/watch?v=4GpWA_hmRhw	01Hrs 54Min 03Hrs 40Min 00Hrs 25Min 10Hrs 25Min 01Hrs 51Min 02Hrs 48Min 10Hrs 17Min
Web References		

LAB Course Code: BECVL0653	LAB Course Name: Industrial PCB & Circuit Engineering Lab	L	T	P	C
Course Offered in: ECE		**0**	**0**	**4**	**2**

Pre-requisite: Basic Electric and Electronic Circuit Components

Course Objectives:

This course provides a comprehensive understanding of PCB materials, manufacturing processes, and fabrication techniques used in electronic system design. It develops practical skills in schematic capture, PCB layout design using KiCad, fabrication file generation, and PCB assembly, testing, and troubleshooting for reliable circuit implementation.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Explain various types of PCB materials, structures, and soldering techniques.	K2
CO2	Apply Ki-Cad software tools for schematic capture and PCB design.	K3
CO3	Design PCB layouts and generate artwork for electronic circuits.	K4
CO4	Perform PCB fabrication processes including etching, drilling, and soldering.	K3
CO5	Assemble, test, and troubleshoot fabricated PCB circuits.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	-	-	-	3	-	-	-	-	-	3	2	2	3
CO2	2	-	-	-	3	-	-	-	-	-	3	2	2	3
CO3	2	-	-	-	3	-	-	-	-	-	3	2	2	3
CO4	2	-	-	-	3	-	-	-	-	-	3	2	2	3
CO5	2	-	-	-	3	-	-	-	-	-	3	2	2	3

List Of Practical's (Indicative & Not Limited To)

S. No.	Objective	CO
1.	Study and identification of various types of Printed Circuit Boards (PCB).	**CO1**
2.	Study and practice of different soldering techniques for electronic components.	**CO1**
3.	Introduction to PCB design software using KiCad.	**CO1**
4.	Creation of schematic diagrams for basic electronic circuits.	**CO2**
5.	Assignment of component footprints and netlist generation.	**CO2**
6.	Design and layout of single-layer PCB.	**CO2**
7.	Design and layout of double-layer PCB	**CO3**
8.	Preparation of PCB artwork and printing process.	**CO3**
9.	Fabrication of PCB using etching and drilling techniques.	**CO3**
10.	Soldering, assembly, and testing of fabricated PCB circuits.	**CO4**
11.	Design and simulation of a regulated power supply PCB circuit using KiCad.	**CO5**
12.	PCB inspection, continuity testing, and troubleshooting of fabricated electronic circuits.	**CO5**

Total Hours: 30 hrs.

LAB Course Code: BECVL0651	LAB Course Name: Low Power VLSI Design Lab	L	T	P	C
Course Offered in: ECE / EE (VLSI)		0	0	4	2

Pre-requisite: CMOS circuit operation and power dissipations

Course Objectives:

This course provides an understanding of power dissipation mechanisms in CMOS circuits and introduces low-power design techniques for combinational and sequential logic optimization. It covers leakage power reduction methods, low-power RTL design strategies, and energy-efficient architectures to achieve improved performance with reduced power consumption.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Analyze and measure static, dynamic, and short-circuit power dissipation components in CMOS logic circuits using electronic simulation tools	**K4**
CO2	Design and optimize combinational and sequential logic blocks for minimal Power-Delay Product (PDP) using alternative logic styles	**K4**
CO3	Implement and evaluate leakage reduction methodologies including MTCMOS, power gating, and transistor stacking configurations	**K4**
CO4	Synthesize and validate low-power RTL-level architectures using clock-gating, multi-voltage domains, and energy-efficient multiplier algorithms.	**K4**

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	2	3	-	-	-	-	-	-	2	3	2
CO2	3	3	2	2	3	-	-	-	-	-	-	2	3	2
CO3	3	3	2	2	3	-	-	-	-	-	-	2	3	2
CO4	3	3	2	2	3	-	-	-	-	-	-	2	3	2

List Of Practical's (Indicative & Not Limited To)

S. No.	Objective	COs
1.	Analyze CMOS inverter power characteristics using Voltage Transfer Characteristics (VTC) and evaluate short-circuit, static, and dynamic power dissipation mechanisms.	**CO1**
2.	Design 2-input NAND and NOR gates using Static CMOS and Pass Transistor Logic (PTL), and compute and compare their Power Delay Product (PDP) performance.	**CO1**
3.	Implement a 1-bit Full Adder using Conventional CMOS, Transmission Gate (TG), and compare total power consumption.	**CO1**
4.	Design D Flip-Flop and JK Flip-Flop circuits and analyze energy consumption under varying clock frequencies.	**CO2**
5.	Simulate a 6T SRAM bit cell and implement techniques for reducing write-driver power consumption.	**CO2**
6.	To design an adiabatic logic inverter circuit.	**CO2**
7.	To design CMOS logic circuits using Low-Vt and High-Vt transistors.	**CO3**
8.	Implement PMOS header or NMOS footer sleep transistors and measure leakage reduction during sleep mode.	**CO3**
9.	To apply forward and reverse body bias voltages to MOS transistors and study their effects on threshold voltage variation and leakage current reduction in CMOS circuits.	**CO3**

10.	To design and implement clock gating logic in a synchronous register circuit and evaluate the reduction in dynamic power consumption using simulation and power analysis tools.	**CO4**
11.	To design a conventional array multiplier. And to implement bypass or row-switching techniques for low-power operation.	**CO4**
12.	To implement Dynamic Voltage Scaling (DVS) techniques in CMOS circuits and study the effect of supply voltage variation on circuit delay, power consumption, and overall energy efficiency.	**CO4**
		Total Hours: 30 hrs.

LAB Course Code: BEC0612P	LAB Course Name: Image Processing and Pattern Recognition Lab	L	T	P	C
Course Offered in: B.Tech. ECE		0	0	2	1

Pre-requisite: Python/MATLAB, Probability, Image Processing Fundamentals.

Course Objectives:

The course aims to provide fundamental knowledge of image enhancement, sharpening, restoration, compression, and segmentation techniques in digital image processing. It enables students to analyze spatial and texture features of images and apply various enhancement and segmentation methods for image analysis and computer vision applications.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Implement image sharpening and image enhancement algorithm.	K3
CO2	Analyze the power of various image restoration and compression techniques.	K4
CO3	Learn basic skills for image segmentation and image analysis.	K2
CO4	Analyze the spatial/ texture features of image.	K4
CO5	Implement and evaluate different enhancement and segmentation techniques for developing computer vision applications.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	-	3	-	-	-	-	3	2	2	2	2
CO2	2	2	2	-	3	-	-	-	-	3	2	2	2	3
CO3	2	2	2	-	3	-	-	-	-	3	2	2	2	3
CO4	2	2	2	-	3	-	-	-	-	3	2	2	2	3
CO5	2	2	2	-	3	-	-	-	-	3	2	2	2	3

List Of Practical's (Indicative & Not Limited To)		**CO**
1	Write a program using MATLAB/Python to display grey scale/color images.	**CO1**
2	Write a program using MATLAB/Python to extract different attributes (i.e., Geometrical and texture) of an Image.	**CO4**
3	Write a program using MATLAB/Python for Image Negation.	**CO2**
4	Write a program using MATLAB/Python for Power Law Transformation.	**CO1**
5	Write a program using MATLAB/Python for Histogram Mapping and Equalization.	**CO3**
6	Write a program using MATLAB/Python for Image Smoothening and Sharpening.	**CO1**
7	Write a program using MATLAB/Python for Edge Detection using Sobel, Prewitt and Roberts Operators.	**CO3**
8	Write a program using MATLAB/Python for Morphological Operations on Binary Images	**CO4**
9	Write a program using MATLAB/Python for Pseudo Coloring.	**CO5**
10	Write a program using MATLAB/Python for the segmentation using watershed transform.	**CO5**
11	Write a program to eliminate the high frequency components of an image. Write a MATLAB program for DCT based image compression.	**CO2**
12	Write a program using MATLAB/Python to extract the image features for image segmentation using DWT Computation.	**CO5**

Total Hours: 15 hrs.

LAB Course Code: BEC0616P	LAB Course Name: Real Time Operating System Lab	L	T	P	C
Course Offered in: B. Tech ECE		0	0	2	1

Pre-requisite: Microcontroller architecture, GPIO, timers, serial communication protocols

Course Objectives:

This course provides hands-on experience in developing real-time embedded applications using RTOS platforms such as FreeRTOS, CMSIS-RTOS, and RTX. It covers task scheduling, inter-task communication, synchronization mechanisms, and resource management, enabling students to design, implement, test, and validate RTOS-based applications on ARM Cortex-M and STM32 embedded systems.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Develop and execute RTOS-based programs involving task creation, scheduling, and inter-task communication using appropriate development tools.	K3
CO2	Implement synchronization and resource-sharing mechanisms such as semaphores, mutexes, message queues, and event flags in real-time applications.	K3
CO3	Implement real-time applications using an RTOS like CMSIS-RTOS, Free RTOS, or RTX.	K3
CO4	Perform hands-on experimentation on real or simulated embedded hardware (e.g., STM32, ARM Cortex-M).	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	-	3	-	-	-	-	-	2	2	2	2
CO2	2	2	2	-	3	-	-	-	-	-	2	2	2	2
CO3	2	2	2	-	3	-	-	-	-	-	2	2	2	2
CO4	2	2	2	-	3	-	-	-	-	-	2	2	2	-

List Of Practical's (Indicative & Not Limited To)

S. No.	Objective	CO
1	Setup of toolchain (e.g., Keil uVision, STM32CubeIDE), Introduction to CMSIS-RTOS or FreeRTOS. Blinking LED without RTOS vs. with RTOS.	CO1
2	Create multiple tasks with different priorities; demonstrate task switching and preemption	CO1
3	Use osDelay, vTaskDelay, and timers. Measure task execution time.	CO2
4	Change task priorities dynamically and observe scheduling behavior.	CO2
5	Use binary and counting semaphores for task synchronization	CO3
6	Implement inter-task communication using message queues	CO3
7	Use mailboxes or event flags for signaling between tasks	CO3
8	Use software timers for delayed and periodic task execution	CO4
9	Explore static and dynamic memory allocation APIs in RTOS.	CO4
10	Implement Round Robin, Rate Monotonic (RM), or Earliest Deadline First (EDF) scheduling.	CO4

Total Hours: 15 hrs.

LAB Course Code: BECVL0611P	LAB Course Name: OLED and QLED Lab	L	T	P	C
Course Offered in: B.Tech. EE (VLSI)		0	0	2	1

Pre-requisite: Basic understanding of electronic devices.

Course Objectives:

This course introduces the fundamentals of modern display technologies, including OLED and QLED devices, their operating principles, materials, fabrication processes, and performance characteristics. It develops skills in display device and pixel circuit design, performance evaluation, and simulation, while exploring emerging technologies such as flexible displays, Micro-LEDs, AR/VR displays, and wearable electronic systems.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Demonstrate the working principles and performance characteristics of modern display technologies including OLED and QLED systems.	K3
CO2	Analyze photometric and colorimetric parameters such as luminance, contrast ratio, Color gamut, and CIE characteristics of display devices.	K3
CO3	Design and simulate OLED/QLED device structures, AMOLED pixel circuits, and compensation techniques using modern CAD/simulation tools.	K4
CO4	Evaluate fabrication methods, material properties, efficiency metrics, and reliability issues associated with OLED and QLED technologies.	K4
CO5	Investigate advanced display technologies including flexible displays, Micro-LEDs, AR/VR displays, and wearable electronic applications.	K5

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	-	3	-	-	-	-	-	-	2	2	2
CO2	2	2	2	-	3	-	-	-	-	-	-	2	2	2
CO3	2	2	2	-	3	-	-	-	-	-	-	2	2	2
CO4	2	2	2	-	3	-	-	-	-	-	-	2	2	2
CO5	2	2	2	-	3	-	-	-	-	-	-	2	2	2

List Of Practical's (Indicative & Not Limited To)

S. No.	Objective	CO
1	Study and comparative analysis of CRT, LCD, LED, OLED, and QLED display technologies based on luminance, contrast ratio, viewing angle, response time, and power consumption.	CO1
2	Measurement and analysis of photometric parameters such as luminance, brightness, colour temperature, and contrast ratio using display characterization tools.	CO1
3	Simulation and plotting of CIE chromaticity diagram and colour gamut analysis for OLED and QLED displays using MATLAB/Python.	CO1
4	Study of OLED device operation by simulating charge injection, carrier transport, and electron-hole recombination characteristics.	CO2
5	Design and simulation of PMOLED and AMOLED pixel architectures and comparison of their driving mechanisms and display performance.	CO2
6	Characterization of OLED material layers including ITO anode, HTL, ETL, cathode, and emissive layer using energy band diagrams and device simulation tools.	CO2

7	Simulation-based extraction of OLED efficiency parameters including Internal Quantum Efficiency (IQE) and External Quantum Efficiency (EQE).	**CO3**
8	Study of OLED fabrication techniques such as Vacuum Thermal Evaporation (VTE), Inkjet Printing, and encapsulation methods through process flow analysis.	**CO3**
9	Design and simulation of AMOLED pixel driving circuits including 2T1C, 5T1C, and 7T1C compensation circuits using MATLAB	**CO4**
10	Analysis of threshold voltage variation and implementation of compensation techniques in AMOLED pixel circuits using LTPS and IGZO TFT backplanes.	**CO4**
11	Study of Quantum Dot (QD) characteristics including quantum confinement effect and size-dependent emission spectrum analysis for QLED applications.	**CO5**
12	Comparative analysis of OLED, QLED, and Micro-LED technologies for AR/VR, wearable electronics, and flexible display applications based on efficiency, colour purity, reliability, and lifetime.	**CO5**
		Total Hours: 15 hrs.

Course Code: BECVL0654	Course Name: AI and ML for VLSI (Workshop mode)	L	T	P	C
Course Offered in: B.Tech. EE (VLSI)		0	0	6	3

Pre-requisite: Basics of VLSI Process Technologies, Testing & Testability

Course Objectives:

This course introduces the fundamentals of machine learning and its applications in VLSI design and semiconductor systems. It develops practical skills in scripting, automation, and CAD workflows while exploring machine learning techniques for physical design, fabrication optimization, logic synthesis, testing, verification, and reliability analysis.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Explain the fundamentals of machine learning algorithms and their applications in engineering systems	K2
CO2	Apply scripting concepts, shell programming, operating system fundamentals, and version control processes for automation tasks.	K3
CO3	Analyze the scope and taxonomy of machine learning techniques in VLSI physical design and CAD optimization.	K4
CO4	Evaluate machine learning approaches for semiconductor fabrication, lithographic modeling, mask optimization, and yield enhancement.	K5
CO5	Develop understanding of machine learning applications in logic synthesis, testing, verification, and aging analysis of VLSI systems.	K4

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	2	2	2	-	-	-	-	-	-	-	-	2	2	3
CO2	2	2	2	-	-	-	-	-	-	-	-	2	2	3
CO3	2	2	2	-	-	-	-	-	-	-	-	2	2	3
CO4	2	2	2	-	-	-	-	-	-	-	-	2	2	3
CO5	2	2	2	-	-	-	-	-	-	-	-	2	2	3

Course Contents / Syllabus

Unit 1	**Fundamentals of Machine Learning**	**09 hours**

Introduction to Machine Learning, Aims and Applications of Machine Learning, Supervised and Unsupervised Learning, Linear Regression, Logistic Regression, Instance-Based Learning, Bayesian Learning, Support Vector Machine (SVM), Kernel Functions and Applications.

Unit 2	**Learning Algorithms and Scripting Concepts**	**09 hours**

Introduction to Learning Algorithms, Scripting Concepts and Automation, Shell Responsibilities, Operating System Fundamentals, Hardware, Kernel and File System, Passing Arguments and Environment Variables, Process Management, Networking Concepts, Version Control Processes and Tools.

Unit 3	**Machine Learning in VLSI Design**	**09 hours**

Taxonomy for Machine Learning in VLSI Design, Scope of Machine Learning in VLSI Physical Design, Data-Driven Design Methodologies, Machine Learning Assisted CAD Tools, Optimization Techniques in Physical Design.

Unit 4	**Machine Learning for Fabrication and Physical Design**	**09 hours**

Machine Learning for Semiconductor Fabrication Lithographic Process Models Mask Optimization Techniques Physical Design Automation Yield Enhancement Techniques using Machine Learning Defect Prediction and Process Variation Analysis.

Unit 5	**Machine Learning for Verification, Testing and Reliability**	**09 hours**

Machine Learning in Logic Synthesis, Physical Verification Techniques, Testing and Fault Diagnosis, Machine Learning-Based Aging Analysis, Reliability and Lifetime Prediction, Future Trends in AI-Assisted VLSI Design.		
		Total Lecture Hours | **45 hours**
Textbook:		
		Authors Name
1. Introduction to Machine Learning, MIT Press, 4th Edition, 2020.		Ethem Alpaydın.
2.Machine Learning for VLSI Computer-Aided Design, Springer International Publishing, 2022.		Andrew B. Kahng
Reference Books:		
		Authors Name
1. Pattern Recognition and Machine Learning, Springer, 2006.		Christopher M. Bishop
2. CMOS VLSI Design: A Circuits and Systems Perspective, Pearson Education, 2015.		Neil H. E. Weste and David Money Harris.
Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	https://youtu.be/YLczBemZpaE?si=wJCdoUed7epj52H9 https://youtu.be/TBgFgwOBqCA?si=ZIxAbq2niwEFXORj https://youtu.be/qJ_bXhrUOkc?si=iLgeb2zAcQPsfyBy https://youtu.be/WfZeeDzV2Tw?si=9gBraUjM2f94bOg4 https://youtu.be/xXk3WiPGux8?si=jPueaS99ftUyKZEH https://youtu.be/bor0qLifjz4?si=iDQwBClGx9XvASjW https://youtu.be/KVhDnP_cquw?si=EsOyDyeQI9Ztm0KO	00Hrs 27Min 01Hrs 53Min 02Hrs 38Min 10Hrs 07Min 00Hrs 25Min 01Hrs 21Min 02Hrs 48Min
Web References		

List of Practical

S. No.	Name of Experiments/ Programs	CO
1	Implement and compare Linear Regression and Logistic Regression models using Python/Scikit-Learn on a semiconductor manufacturing dataset. Analyze prediction accuracy and error metrics.	CO1
2	Develop a K-Nearest Neighbor (Instance-Based Learning) model for wafer defect classification and evaluate the impact of different values of K.	CO1
3	Implement a Naïve Bayes Classifier for chip fault classification and analyze classification performance using confusion matrix and ROC curves.	CO1
4	Design and evaluate a Support Vector Machine (SVM) model for process variation classification using different kernel functions (Linear, Polynomial, RBF).	CO2
5	Perform Unsupervised Learning using K-Means Clustering to identify patterns in fabrication process parameters and analyze cluster quality.	CO2
6	Create shell scripts for automating data preprocessing, feature extraction, and model training workflows in a Linux environment.	CO2
7	Analyze process management and resource utilization during machine learning model training using Linux commands and shell scripting tools.	CO3
8	Implement a version-controlled machine learning project using Git and analyze collaborative development workflows for VLSI CAD applications.	CO3

9	Develop a machine learning-based framework for predicting wirelength in VLSI physical design using regression techniques.	**CO3**
10	Analyze placement optimization data and apply machine learning algorithms to improve placement quality metrics in VLSI design.	**CO4**
11	Implement a lithography hotspot detection model using supervised machine learning and evaluate prediction accuracy.	**CO4**
12	Develop a machine learning model for semiconductor yield prediction using fabrication process datasets and analyze influential process parameters.	**CO4**
13	Perform defect prediction and process variation analysis using classification algorithms and compare model performance.	**CO5**
14	Design a machine learning-based fault diagnosis system for digital circuits and evaluate testing coverage and diagnostic accuracy.	**CO5**
15	Implement reliability prediction and aging analysis of VLSI circuits using regression/classification techniques and analyze lifetime estimation results.	**CO5**
	Total Hours	**35**