NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY GREATER NOIDA GAUTAM BUDDH NAGAR

(An Autonomous Institute)

Affiliated to

Dr. A.P.J. ABDUL KALAM TECHNICAL UNIVERSITY, UTTAR PRADESH LUCKNOW

Evaluation Scheme & Syllabus

For

Bachelor of Technology

Electronics Engineering (VLSI Design and Technology)

Second Year

(Effective from the Session: 2026-27)

NOIDA INSTITUTE OF ENGINEERING & TECHNOLOGY, GREATER NOIDA
(An Autonomous Institute)

B. TECH (EE-VLSI)
Evaluation Scheme
SEMESTER III

S. No.	Subject Codes	Subject Name	Types of Subjects	Periods			Evaluation Schemes				End Semester		Total	Credit
				L	T	P	CT	TA	TOTAL	PS	TE	PE		
1	CCSCC00301	Employability Skill Development - I	Mandatory	2	0	0	60	40	100				100	2
2	CECVL0301	Analog Digital Signal Processing & Communication	Mandatory	2	0	0	30	20	50		50		100	2
3	CECVL0303	Embedded Computing Principles	Mandatory	3	0	0	30	20	50		100		150	3
4	CECVL0304	VLSI Technology	Mandatory	2	0	0	30	20	50		50		100	2
5	CECVL0302	CMOS Digital Integrated Circuit	Mandatory	3	0	0	30	20	50		100		150	3
6	CASL0301	Technical Communication	Mandatory	2	0	0	30	20	50		50		100	2
7	CECVL0353	Embedded Computing Principles Lab	Mandatory	0	0	4				50		50	100	2
8	CECVL0351	Analog Digital Signal Processing and Communication Lab	Mandatory	0	0	4				50		50	100	2
9	CECVL0352	CMOS Digital Integrated Circuit Lab	Mandatory	0	0	2				25		25	50	1
10	CEC0355	Verilog-HDL	Mandatory	0	0	6				50		100	150	3
11	CEC0359	Internship-I	Mandatory	0	0	2				50			50	1
12	CNC0301 / CNC0302	Artificial Intelligence and Cyber Ethics/Environmental Science	Compulsory Audit	2	0	0	30	20	50				50	NA
		*Massive Open Online Courses (For B. Tech Hons. Degree)	*MOOCs											
			TOTAL	**17**	**1**	**18**	**210**	**140**	**350**	**225**	**400**	**225**	**1150**	**23**

* List of MOOCs (Infosys Springboard) Based Recommended Courses for Second year B. Tech Students

S. No.	Subject Code	Course Name	University/ Industry Partner Name	N. of Hours	Credits
1.	CMC0015	Data Structures and Algorithms using Python - Part 1	Infosys Wingspan (Infosys Springboard)	29h 27m	2
2.	CMC0038	Express PCB Training	IIHT	15h 6m	1
3.	CMC0015	Data Structures and Algorithms using Python - Part 1	Infosys Wingspan (Infosys Springboard)	29h 27m	2

PLEASE NOTE: -

- **A 3-4 weeks Internship shall be conducted during summer break after semester-II and will be assessed during semester-III**
- **Compulsory Audit (CA) Courses (Non-Credit - CNC0301/CNC0302)**
  - All Compulsory Audit Courses (a qualifying exam) do not require any credit.
  - The total and obtained marks are not added in the grand total.

Abbreviation Used:

L: Lecture, T: Tutorial, P: Practical, CT: Class Test, TA: Teacher Assessment, PS: Practical Sessional, TE: Theory End Semester Exam, CE: Core Elective, OE: Open Elective, DE: Departmental Elective, PE: Practical End Semester Exam, CA: Compulsory Audit, MOOCs: Massive Open Online Courses.

NOIDA INSTITUTE OF ENGINEERING & TECHNOLOGY, GREATER NOIDA
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B. TECH (EE-VLSI)
Evaluation Scheme
SEMESTER IV

S. No.	Subject Codes	Subject Name	Types of Subjects	Periods			Evaluation Schemes				End Semester		Total	Credit
				L	T	P	CT	TA	TOTAL	PS	TE	PE		
1	CASCC0401	Employability Skill Development -II	Mandatory	2	0	0	60	40	100				100	2
2	CAS0403	Advanced Engineering Mathematics	Mandatory	3	1	0	30	20	50		100		150	4
3	CECVL0401	Low Power VLSI Design	Mandatory	2	0	0	30	20	50		50		100	2
4	CEC0401	CMOS Analog Integrated Circuit	Mandatory	3	0	0	30	20	50		100		150	3
5	CECVL0402	Product Architecture Models and Firmware	Mandatory	3	0	0	30	20	50		100		150	3
6		Departmental Elective-I	Departmental Elective	3	0	0	30	20	50		100		150	3
7	CECVL0451	Low Power VLSI Design Lab	Mandatory	0	0	4				50		50	100	2
8	CEC0451	CMOS Analog Integrated Circuit Lab	Mandatory	0	0	2				25		25	50	1
9	CECVL0455	VLSI Principles, RTL Design and Verification	Mandatory	0	0	6				50		100	150	3
10	CEC0459	Mini Project	Mandatory	0	0	2				50		50	50	1
11	CSCC0452	Problem Solving Approaches	Mandatory	0	0	2				50			50	1
12	CNC0402 / CNC0401	Environmental Science/ Artificial Intelligence and Cyber Ethics	Compulsory Audit	2	0	0	30	20	50		50		50	NA
		Massive Open Online Course (For B. Tech. Hons. Degree)	*MOOCs											
		TOTAL		**17**	**0**	**16**	**210**	**140**	**350**	**225**	**400**	**175**	**1200**	**25**

*** List of MOOCs (Infosys Springboard) Based Recommended Courses for Second year B. Tech Students**

S. No.	Subject Code	Course Name	University/ Industry Partner Name	N. of Hours	Credits
1.	CMC0061	Internet of Things 201	Infosys Wingspan (Infosys Springboard)	15h 59m	1
2.	CMC0062	IoT Raspberry Pi with Projects	IIHT	12h 25m	0.5
3.	CMC0063	Mobile Apps Development - Advanced Applications	IIHT	14h 23m	1

PLEASE NOTE: -

- **A 3-4 weeks Internship shall be conducted during summer break after semester-IV and will be assessed during Semester-V**
- **Compulsory Audit (CA) Courses (Non-Credit - CNC0401/CNC0402)**
  - All Compulsory Audit Courses (a qualifying exam) do not require any credit.
  - The Total and obtained marks are not added in the Grand Total.

Abbreviation Used:

L: Lecture, T: Tutorial, P: Practical, CT: Class Test, TA: Teacher Assessment, PS: Practical Sessional, TE: Theory End Semester Exam, CE: Core Elective, OE: Open Elective, DE: Departmental Elective, PE: Practical End Semester Exam, CA: Compulsory Audit, MOOCs: Massive Open Online Courses.

List of Department Elective:

S. No.	Subject Code	Subject Name	Bucket Name	Semester
1	CEC0411	Data Analytics	Artificial Intelligence	IV
2	CEC0412	Sensor Technologies	IoT	IV

NOIDA INSTITUTE OF ENGINEERING & TECHNOLOGY, GREATER NOIDA
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AICTE Guidelines in Model Curriculum:

A student will be eligible to get Under Graduate degree with Honours only, if he/she completes the additional MOOCs courses such as Infosys Springboard/NASSCOM/CISCO (as applicable) certifications, or any other online courses recommended by the Institute (Equivalent to 20 credits). During Complete B.Tech. Program Guidelines for credit calculations are as follows.

1. For 6 to 12 Hours =0.5 Credit
2. For 13 to18 =1 Credit
3. For 19 to 24 =1.5 Credit
4. For 25 to 30 =2 Credit
5. For 31 to 35 =2.5 Credit
6. For 36 to 41 =3 Credit
7. For 42 to 47 =3.5 Credit
8. For 48 and above =4 Credit

For registration to MOOCs Courses, the students shall follow Infosys Springboard/NASSCOM/CISCO (as applicable) registration details as per the assigned login and password by the Institute these courses may be cleared during the B. Tech degree program (as per the list provided). After successful completion of these MOOCs courses, the students shall provide their successful completion status/certificates to the Controller of Examination (COE) of the Institute through their coordinators/Mentors only.

The students shall be awarded Honours Degree as per following criterion.

i. If he / she secures 7.50 as above CGPA.

ii. Passed each subject of that degree program in the single attempt without any grace.

iii. Successful completion of MOOCs based 20 credits

Course Code: CCSCC00301	Course Name: Employability Skill Development - I	L	T	P	C
Course Offered in: ECE / EE (VLSI)		2	0	0	2

Pre-requisite: Reasoning and Basic Programming

Course Objectives:

Section A: Develop understanding of computer systems, mathematical foundations, and programming concepts while applying structured problem-solving techniques to design logical solutions effectively.
Section B: Enhance numerical ability and logical reasoning skills through speed mathematics, number systems, and analytical problem-solving techniques for competitive aptitude development.
Section C: To develop the ability to communicate effectively and empathetically in workplace situations while strengthening active listening, adaptability, and cross-cultural awareness for navigating complex professional environments.

Course Outcome:		Bloom's Level
CO1	Apply fundamental concepts of computer systems, mathematical foundations, and programming constructs to analyze and solve basic computational problems.	K3
CO2	Design and develop structured solutions for problem statements by applying SDLC principles, logical thinking, and flowchart/pseudocode techniques.	K6
CO3	Apply fundamental number theory concepts such as divisibility, HCF & LCM, remainder theorem, and cyclicity to solve quantitative problems efficiently	K3
CO4	Solve problems involving logical reasoning and analytical thinking, including direction sense, blood relations, series patterns, and time-based puzzles like clocks and calendars.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	-	2	3	1	-	3	2	2	2	-	-	-
CO2	3	3	3	3	3	2	1	3	2	2	2	-	-	-
CO3	3	3	2	1	-	-	-	1	2	2	2	-	-	-
CO4	-	-	-	-	1	2	-	3	2	2	-	-	-	-

Course Contents / Syllabus

Section-A

Unit 1	**Foundations of Computer Systems and Mathematical Concepts**	**8 hours**

Computer System Fundamentals: Introduction to Assembler, Compiler, Interpreter, Role of Loader and Linker in program execution. **Mathematical Foundations for Computing:** Sets, Relations, and Functions: definitions and applications, Principle of Mathematical Induction and its use in proofs.
Basic Concepts of Programming Language: Memory model of C/C++ Program, Activation Record of a function, L-Value/ R-Value concept. Operators, Precedence, Order of Evaluation and Associativity. Pointers and Dynamics Memory Concept, Functions (argument passing, concept of scope), Understanding Recursion, Bitwise Operations.

Unit 2	**Design and develop structured solutions for problem statements**	**8 hours**

Introduction to Software Development Life Cycle, Step-by-step solution to simple problems, Developing logic/flowchart/pseudocode. Step-wise refinement and Procedural Abstraction.
Case Study*: Understand the problem statement, identify a feasible solution, and develop the logic along with a flowchart for the proposed solution.

Section-B

Unit 3:	**Speed Math and Number System**	**8 hours**

Classification of number, Divisibility Rule, Factorization, HCF & LCM, It's Application, Unit digit (Cyclicity), Last two-digit, Remainder theorem, Factorial and Number of zeroes, Highest power		
Unit 4	**Analytical and Logical Reasoning**	**6 hours**
Direction and Sense, Blood Relation, Number Series and Letter Series, Coding Decoding.		
		Total Lectures: 30 hours

**A list of problem statements will be provided by the mentor; you may choose any one.*
Note: *Students may choose an alternative problem statement with prior approval from the mentor.*

Reference Books:

S. No	Book Title	Author
1.	A Project-Based Introduction to Programming	Access Point Publishing
2.	Programming: Principles and Practice Using C++	Bjarne Stroustrup
3.	Effective Modern C++	Scott Meyers
4.	Quantitative Aptitude	R S Aggarwal
5.	Verbal & Non-Verbal Reasoning	R S Aggarwal

Mode of Evaluation

CIE							**ESE**	**Total**
ST1	**ST2**	**ST3**	**TA1 10**	**TA2 10**	**TA3 10**	**Attendance 10**		
60			**40**					**100**

Course Code: CECVL0301	Course Name: Analog Digital Signal Processing & Communication	L	T	P	C
Course Offered in: B. Tech.EE (VLSI)		2	0	0	2
Pre-requisite: Basic Knowledge of Mathematical Analysis					
Course Objectives:					
This course introduces the fundamental concepts of signals, systems, and digital signal processing techniques used in communication and signal analysis. It develops the ability to analyze signals in the frequency domain, design digital filters, and understand analog modulation techniques using appropriate signal processing tools and methods.					

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Explain the fundamentals of signal and systems with signal processing.	K2
CO2	Apply Discrete Fourier Transform for Linear Filtering	K3
CO3	Design of digital IIR and FIR filters.	K4
CO4	Explain various modulation and demodulation methods of Amplitude Modulation and Angle Modulation.	K3
CO5	Explain various digital modulation, demodulation techniques and communication Protocol	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	-	-	-	-	-	-	-	-	1	2	1
CO2	3	3	2	-	-	-	-	-	-	-	-	1	3	1
CO3	3	3	3	-	-	-	-	-	-	-	-	1	3	1
CO4	3	2	1	-	-	-	-	-	-	-	-	1	3	1
CO5	3	3	2	-	-	-	-	-	-	-	-	1	3	1

Course Contents / Syllabus

Unit 1	**Signal and System**	**8 hours**
Classification of Signals: Unit step, Unit impulse and Unit ramp functions; Exponential and sinusoidal signals; Periodic and Aperiodic Signals, Energy and Power Signals, Even and Odd Signals, Causal, Anti-causal and Non-Causal Signals. Classification of systems: Analog and Digital Systems, Linear and Nonlinear systems, Time varying and Time-invariant systems, causal and non-causal systems, stability of linear time invariant systems		
Unit 2	**Signal processing**	**6 hours**
Introduction to Analog Signal Processing and Digital Signal Processing, Discrete Fourier Transform (DFT), Inverse DFT, DFT as linear transformation, Twiddle Factor, Circular convolution, Linear filtering using circular convolution, Fast Fourier transform: DIT-FFT algorithm		
Unit 3	**Digital Filter Design**	**6 hours**
Infinite Impulse Response (IIR) filter: Design of IIR Filter using impulse invariant and Bi linear transformation method, Analog and Digital Frequency Transformation, Design of all pole filters, Finite Impulse Response (FIR) filter: Frequency response of linear phase filter, Designing of FIR filter using Fourier series and window techniques		
Unit 4	**Fundamentals of Analog Communication Systems**	**4 hours**

<table>
<tr><td colspan="4">Introduction to Communication system, Need for modulation, Amplitude Modulation and Demodulation, Angle Modulation: Frequency Modulation and Demodulation, Frequency Division Multiplexing (FDM)</td></tr>
<tr><td>Unit 5</td><td colspan="2">Digital Communication and Communication Protocols</td><td>6 hours</td></tr>
<tr><td colspan="4">Sampling Theorem, Pulse Code Modulation (PCM), Line coding, Binary ASK, FSK & PSK Modulation and Demodulation, Differential phase shift keying (DPSK), Quadrature phase shift keying (QPSK). Need and role of protocols, OSI layer, Basic Communication Protocols: IP, UDP, TCP</td></tr>
<tr><td colspan="3">Total Lecture Hours</td><td>30 hours</td></tr>
<tr><td colspan="4">Textbook:
1. John G Prokias, Dimitris G Manolakis, “Digital signal processing Principles Algorithms & Applications”, 4th edition, Pearson education, 2007
2. Herbert Taub and Donald L. Schilling, “Principles of Communication Systems”, Tata McGraw Hill</td></tr>
<tr><td colspan="4">Reference Books:
B.P. Lathi, “Modern Digital and Analog communication Systems”, 4th Edition, Oxford University Press,2010.</td></tr>
<tr><td colspan="2">Self-Study Content Links:</td><td colspan="2">Duration (in Hrs)</td></tr>
<tr><td>MOOCs</td><td></td><td colspan="2"></td></tr>
<tr><td>Video Lectures</td><td>Unit 1
https://youtu.be/CXFtbpYaBXw
Unit 2
https://youtu.be/iBGgzrvwFi8
Unit 3
https://youtu.be/iBGgzrvwFi8
Unit 4
https://youtu.be/iBGgzrvwFi8?si=yISnwWWyqQMYkV2w
Unit 5
https://www.youtube.com/watch?v=4GpWA_hmRhw</td><td colspan="2">
00Hrs 41Min

00Hrs 25Min

00Hrs 25Min

00Hrs 25Min

00Hrs 28Min</td></tr>
<tr><td>Web References</td><td></td><td colspan="2"></td></tr>
</table>

Course Code: CECVL0303	Course Name: Embedded Computing Principles	L	T	P	C
Course Offered in: B. Tech EE (VLSI)		3	0	0	3

Pre-requisite: Basic Knowledge of Mathematical Analysis

Course Objectives:

This course introduces the fundamental concepts, functions, and architectures of controllers used in industrial automation and control systems. It develops the ability to design, program, and implement controller-based solutions for monitoring and control applications, while evaluating their performance, reliability, and integration in real-world automated systems.

Course Outcome: After completion of the course, the student will be able to		Bloom's Level
CO1	Interpret controller functions.	K2
CO2	Map functions of controller with Architecture.	K2
CO3	Program the controller functionalities.	K4
CO4	Apply the requirements of expected controller solutions.	K3
CO5	Infer overall system engineering of controllers.	K2

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	1	-	-	-	-	-	-	-	2	2	3
CO2	3	3	2	1	-	-	-	-	-	-	-	3	3	3
CO3	3	3	3	-	-	-	-	-	-	-	-	3	3	3
CO4	3	3	3	3	-	-	-	-	-	-	-	3	3	3
CO5	3	3	3	3	-	-	-	-	-	-	-	3	3	3

Course Contents / Syllabus

Unit 1	Fundamentals of 8-bit Microprocessors and 8051 Microcontroller Programming	10 hours

Fundamentals of 8-bit microprocessor, Introduction and fundamentals of 8051 microcontroller, Pin Diagram, Functional block diagram and memory organization, I/O interfacing, Timer and Counter, Serial communication, Interrupts Addressing Modes, Programming with 8051 microcontroller, Programmable peripheral interfaces, I/O programming Debugging principles, Applications

Unit 2	AVR Microcontrollers: Architecture, Programming, and Interfacing	8 hours

Introduction to AVR microcontroller and architecture, AVR memory organization, Peripheral interfaces, IDEs for AVR Basic Programs using AVR, Interfacing I/O devices and Sensors, PWM configuration, ADC configuration - Use cases

Unit 3	Programming and Embedded C Fundamentals	8 hours

Introduction to C programming, C based simple programs, Basics of Embedded C, Data types, Conditions, Loop, Arrays Sprintf convert float/int to string in embedded C, Pointers and functions, Passing arrays to functions.

Unit 4	Embedded Development Boards and Applications	10 hours

Fundamentals of development boards and architecture (Arduino UNO, ESP32), Arduino IDE, Smart parking management system, Automatic animal feeder system, Line follower robotics, Pick and place robots, Obstacle sensing autonomous robot, Object identification robot, Truck load object counting systems, Gateway integrated diesel generator monitoring system, Integration of IoT data with cloud

Unit 5	**Cyber Physical System and Embedded Systems**	**9 hours**
Fundamentals of cyber physical system (CPS), Evolution of Processors, ARM Cortex Architecture, Embedded C Programming for ARM Cortex, Interfacing ARM cortex processor with relay, buzzer, 16 x2 LCD, matrix key and stepper motors, Raspberry Pi Pico and Micro Python, Thonny IDE, Sensor interfacing with Raspberry Pi Pico.		
	Total Lecture Hours	**45 hours**
Textbook: 1. J Wayne Wolf, "Computers as Components, Principles of Embedded Computing System Design"		
Reference Books: 1. Frank Vahid & Tony Givargis *"Embedded System Design"* 1st Edition, Wiley 2. Xiaocong Fan "Real-Time Embedded Systems" 1st Edition, Morgan Kaufmann		
Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	**Unit 1** https://youtube.com/playlist?list=PLuv3GM6-gsE01L9yDO0e5UhQapkCPGnY3&si=OHZf4gSCZarUpYp8	00Hrs 29Min
	Unit 2 https://youtu.be/WGcierfsSNo?si=UkiFTNREEjqr3IjG	00Hrs 28Min
	Unit 3 https://youtube.com/playlist?list=PLUQpHm_JtukII_8U9pucV61MX2YE2CSUt&si=a2FXybS5OZo37TMU	00Hrs 35Min 01Hrs 25Min
	Unit 4 https://youtube.com/playlist?list=PLwWF-ICTWmB7-b9bsE3UcQzz-7ipI5tbR&si=sINj71g3ufKuW1vk https://youtu.be/RiYnucfy_rs?si=ydzokWtCaBsv5NRU	00Hrs 09Min 00Hrs 37Min
	Unit 5 https://youtube.com/playlist?list=PLC7Up2560NXvkxDht6GBy9nVP4MR7M5HM&si=4jKW5YCoEHMkPpI7	
Web References		

Course Code: CECVL0304	Course Name: VLSI Technology	L	T	P	C
Course Offered in: B. Tech. EE (VLSI)		2	0	0	2

Pre-requisite: Basic knowledge of Semiconductor materials

Course Objectives:

This course introduces the fundamental processes involved in VLSI fabrication, including semiconductor material growth, oxidation, photolithography, doping, and metallization. It develops an understanding of IC manufacturing technologies and their impact on device performance, reliability, and integrated circuit realization.

Course Outcome: After completion of the course, the student will be able to		Bloom's Level
CO1	Describe the IC fabrication environment, safety practices, and various unit processes involved in VLSI technology.	**K2**
CO2	Demonstrate understanding of semiconductor material growth and oxidation techniques used in device fabrication and evaluate the characteristics of grown epitaxial layers.	**K4**
CO3	Describe pattern transfer methods and thin-film deposition techniques used in semiconductor manufacturing.	**K2**
CO4	Analyze doping techniques and impurity distribution processes in semiconductor fabrication.	**K2**
CO5	Explain metallization processes, metal selection, and interconnect fabrication techniques in VLSI systems.	**K2**

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	–	–	–	–	–	–	–	–	2	2	2
CO2	3	2	3	–	–	–	–	–	–	–	–	2	2	2
CO3	3	2	2	–	–	–	–	–	–	–	–	2	2	2
CO4	3	2	3	–	–	–	–	–	–	–	–	2	2	2
CO5	2	2	2	–	–	–	–	–	–	–	–	2	2	2

Course Contents / Syllabus

Unit 1	**Environment for VLSI Technology**	**6 hours**
Environment for VLSI Technology: Clean room and safety requirements, Wafer cleaning processes. Etching Techniques - Wet and Dry Etching, Introduction to Plasma Etch mechanisms, Reactive Plasma Etching, and its applications		
Unit 2	**Epitaxy**	**6 hours**
Epitaxy: Vapor-Phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation, Oxidation: Growth Kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxides Properties, High k and low k dielectrics for ULSI		
Unit 3	**Lithography**	**6 hours**
Lithography: Optical Lithography, Electron beam lithography, Photo masks, Dielectric and Polysilicon Film Deposition: CVD techniques for deposition of Polysilicon, Silicon Dioxide, Silicon Nitride		
Unit 4	**Diffusion**	**6 hours**

Diffusion: Models of diffusion in solids, Fick’s 1-Dimensional diffusion equation, Diffusion of Impurities in Silicon and Silicon Dioxide, Diffusion Equations, Diffusion Profiles, Diffusion Furnace, Solid, Liquid, and Gaseous Sources. Ion-Implantation: Ion- Implantation Technique, Range Theory, Implantation Equipment			
Unit 5	**Metal film deposition**		**6 hours**
Metal film deposition: Metallization, Metallization Application, Metallization Choices, Failure mechanisms in metal interconnects; multi-level metallization schemes. growth and deposition of various films for use in ULSI. Process integration for NMOS, CMOS and Bipolar circuits; Advanced MOS technologies			
		Total Lecture Hours	**30 hours**

Textbook:

	Authors Name
1. Introduction to microelectronic fabrication	Jaeger, R. C.
2. Physics of semiconductor devices	Sze, S. M., & Kwok, K. N.

Reference Books:

	Authors Name
1. VLSI technology	Sze, S. M
2. Fundamentals of microfabrication	Madou, M. J

Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	Unit 1	
	1. https://youtu.be/PJUNgWmbS9E?si=GRMOkMJ0zYzFEyfn	00Hrs 42Min
	2. https://youtu.be/wSSfOqEQClc?si=5MEoyfdA9_lgJzD9	00Hrs 50Min
	Unit 2	
	1. https://youtu.be/S3e7BHBrOhk?si=tMJkRyL6-ZHCcjyR	00Hrs 50Min
	2. https://youtu.be/tWq2OF3abNI?si=QPsUDTw_L6jqd8Jv	00Hrs 52Min
	3. https://youtu.be/Se-rAo3nioU?si=achbYnInhG1bvL3_	00Hrs 48Min
	4. https://youtu.be/VaIMp-sZe0U?si=ZBDrlxGjMsaDk7Ka	00Hrs 51Min
	Unit 3	
	1. https://youtu.be/v9eGO5OjC8A?si=7xJ3yhoJ0ygbAR-T	00Hrs 52Min
	2. https://youtu.be/pcAEEw2Gadg?si=ohNhLWq49XynAC2k	00Hrs 39Min
	3. https://youtu.be/g3_beYKJqOk?si=SSgl2H4uN7BGJsxD	00Hrs 54Min
	4. https://youtu.be/g3_beYKJqOk?si=jcQzjvD0BP3ZWp_U	00Hrs 54Min
	Unit 4	
	1. https://youtu.be/hMZylm9qbgs?si=dxOwJr4eFbJ7cN3h	00Hrs 54Min
	2. https://youtu.be/XO0gnTxzZoI?si=ELNktE49ZVksua9t	00Hrs 55Min
	3. https://youtu.be/3pYqPCK0p9w?si=WdDlTJkGuP2hgaZj	00Hrs 52Min
	Unit 5	
	1. https://youtu.be/Omf26GtJXCI?si=B-Th46DMwO-FvhyZ	00Hrs 51Min
	2. https://youtu.be/sM2nHyo--zA?si=2lvekVZlChHEbqn8	00Hrs 49Min
	3. https://youtu.be/AFpNn0UhSTY?si=muqzOR2Dj_DZna8z	00Hrs 51Min
Web References		

Course Code: CECVL0302	Course Name: CMOS Digital Integrated Circuit	L	T	P	C
Course Offered in: B. Tech. ECE / EE (VLSI)		3	0	0	3

Pre-requisite: Basis knowledge of MOSFET and Digital Electronics

Course Objectives:

This course introduces the fundamentals of MOS devices and CMOS design principles used in digital integrated circuits. It develops the ability to analyze MOS-based logic circuits, including combinational, sequential, and dynamic logic, and provides an understanding of semiconductor memory architectures and their design considerations.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Explain the basics of MOS device and its current voltage characteristics.	K2
CO2	Explain MOS inverters and its static characteristics.	K3
CO3	Design of Combinational and Sequential MOS logic circuits.	K4
CO4	CO4- Explain and design dynamic logic circuits.	K4
CO5	Describe the concept of semiconductor memories.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	-	-	-	-	-	-	-	-	3	1	2
CO2	3	2	3	-	-	-	-	-	-	-	-	3	2	2
CO3	3	3	2	-	-	-	-	-	-	-	-	3	2	2
CO4	3	1	2	-	-	-	-	-	-	-	-	3	2	2
CO5	3	3	3	-	-	-	-	-	-	-	-	3	2	2

Course Contents / Syllabus

Unit 1	**VLSI Design Flow and CMOS fabrication**	**9 hours**

VLSI Design flow: VLSI Design flow & Y-Chart, MOS Structure, MOS System under external Bias, Structure and Operation of MOSFET, Basic MOS Current-Voltage Characteristics, MOSFET Scaling and Small-Geometry Effect, MOSFET capacitances.

Unit 2	**MOS inverter and Static Characteristics**	**9 hours**

Introduction, Resistive-load Inverter, Inverter with N-type MOSFET load, CMOS inverter: Circuit operation, DC transfer characteristics, Noise margin: calculation of VIL, VIH, Vth, Design of CMOS inverter, Supply voltage scaling, Switching characteristic: Delay time definition, calculation of delay times, Power dissipation of CMOS inverter.

Unit 3	**Combinational and sequential MOS logic circuits**	**9 hours**

Combinational MOS Logic Circuits with Depletion NMOS loads, CMOS Logic circuits, Realizing Boolean expressions using CMOS gates, Complex Logic circuits design, Design of Half Adder, Full Adder, CMOS Transmission Gates (Pass Gates).

Sequential MOS Logic Circuits: Behavior of Bi-stable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D-latch, and edge triggered flip-flop.

<table>
<tr><td>Unit 4</td><td>Dynamic logic Circuits</td><td colspan="2">9 hours</td></tr>
<tr><td colspan="4">Introduction, Basic Principles of Pass Transistor Circuits, Synchronous dynamic circuit techniques: Dynamic Pass Transistor Circuits, CMOS Transmission Gate Logic, High performance Dynamic CMOS Logic Circuits: CMOS Domino Logic, charge sharing problem.</td></tr>
<tr><td>Unit 5</td><td>Introduction to Semiconductor memories and ASIC</td><td colspan="2">9 hours</td></tr>
<tr><td colspan="4">Semiconductor Memories: Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells.</td></tr>
<tr><td colspan="2" align="right">Total Lecture Hours</td><td colspan="2">45 hours</td></tr>
<tr><td colspan="4">Textbook:
1. Kang, Leblebici, “CMOS Digital Integrated Circuits”, TMH, 3rd Edition.
2. Rabaey, Chandrakasan and Nikolic, “Digital Integrated Circuit: A Design Perspective”, PHI; Latest Edition
3. Weste and Eshraghian, “Principles of CMOS VLSI Design” Addison Wesley, Latest Edition.</td></tr>
<tr><td colspan="4">Reference Books:
1. Weste and Harris, “CMOS VLSI Design”. CRC Press, (2002)
2. Bushnell and Agrawal, “Essentials of VLSI Testing for digital, memory and mixed-signal VLSI Circuits”, Kluwer Academic Publishers.</td></tr>
<tr><td colspan="3">Self-Study Content Links:</td><td>Duration (in Hrs)</td></tr>
<tr><td>MOOCs</td><td colspan="2"></td><td></td></tr>
<tr><td>Video Lectures</td><td colspan="2">Unit 1
https://onlinecourses.nptel.ac.in/noc20_ee29/preview
Unit 2
https://www.youtube.com/watch?v=MuBiC9yz2fc
Unit 3
https://www.youtube.com/watch?v=yndN_m9L5qI
Unit 4
https://www.youtube.com/watch?v=UuafwIJAKhY
Unit 5
https://www.youtube.com/watch?v=vD0sNigq1C</td><td>
00Hrs 03Min

00Hrs 49Min

00Hrs 29Min

00Hrs 04Min

00Hrs 22Min</td></tr>
<tr><td>Web References</td><td colspan="2"></td><td></td></tr>
</table>

Course Code: CASL0401	Course Name: Technical Communication	L	T	P	C
Course Offered in: B. Tech. All branches (except CSBS)		**2**	**0**	**0**	**2**
Pre-requisite: Intermediate level and above (CEFR level)					
Course Objectives:					
Demonstrate effective verbal and non-verbal communication skills in diverse professional settings, including meetings, presentations, and interpersonal interactions. Develop and apply clear, concise, and audience-appropriate written communication, such as emails, letters, memos, resume', using correct grammar, tone, and format. Adapt communication style based on cultural, organizational, and situational contexts to foster inclusive and respectful professional relationships. Employ digital communication tools and platforms (e.g., video conferencing, business messaging apps) responsibly and effectively in remote or hybrid work environments.					

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Comprehend the principles and functions of technical communication.	K2
CO2	Write for specific audience and purpose to fulfil the provided brief.	K3
CO3	Recognize and produce different kinds of technical documents.	K3
CO4	Apply effective speaking skills to efficiently carry out official discourses.	K3
CO5	Demonstrate their understanding of communication through digital media.	K3

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	1	1	1	1	1	2	1	2	3	1	1	-	-	-
CO2	1	1	1	1	1	1	1	2	3	1	1	1	-	1
CO3	1	1	1	1	1	1	1	2	3	1	1	1	2	2
CO4	1	1	1	1	1	1	1	2	3	1	1	1	2	2
CO5	1	1	1	1	1	1	1	2	3	1	1	1	1	2

Course Contents / Syllabus		
Unit 1	**Introduction to Technical Communication**	**6 hours**
Definition, Process, Types, Levels, Flow and Barriers to Technical Communication with emphasis on gender neutral language and cultural sensitivity, Significance of audience in technical communication		
Unit 2	**Technical Writing 1**	**6 hours**
Technical writing skill – characteristics, examples, Business letters/emails - Content organization, Tone and intent, Agenda & Minutes of Meetings		
Unit 3	**Technical Writing 2**	**6 hours**
Job application, Resume', Report, proposal, Technical paper – Abstract, Ethical Writing – Copy Editing, Referencing and Plagiarism		
Unit 4	**Public Speaking**	**06 hours**
Components of effective speaking – Simplicity, order, balance in arranging ideas. Importance of *KOPPACT* Appearing for a job interview, FAQs, Telephonic & Online Interviews		
Unit 5	**Virtual/Remote Communication**	**6 hours**
Remote work – online platforms, Video conferencing; Virtual etiquette- email ids, usernames		

Writing Blogs & creating Vlogs	
Total Lecture Hours	**30 Hours**

Textbook:	
	Authors Name
1. Technical Communication – Principles and Practices	Meenakshi Raman & Sangeeta Sharma
Reference Books:	
	Authors Name
1. Technical Communication	John M. Lannon & Laura J. Gurak
2. Spoken English- A Manual of Speech and Phonetics	R K Bansal & J B Harrison
3. Business Correspondence and Report	Prof. R C Sharma, Krishna Mohan, and Virendra Singh Nirban
4. Intercultural Communication in Virtual Exchange	Francesca Helm

Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	**Unit1:** https://onlinecourses.nptel.ac.in/noc24_ge37/preview	00Hrs 05Min
	Unit2: https://archive.nptel.ac.in/courses/109/106/109106094/	
	Unit3: https://www.youtube.com/watch?v=kOJlwMJxEG0&t=8s	00Hrs 37Min
	Unit4: https://www.youtube.com/watch?v=Sg7Q_dC_fWU&list=PLPuC5CMHiqmuzq_KQ4aw0V9Q7xJY6aezb	00Hrs 59Min
	Unit5: https://www.youtube.com/watch?v=ymLFJDpjgCk&list=PLPuC5CMHiqmuzq_KQ4aw0V9Q7xJY6aezb&index=6	00Hrs 56Min

Mode of Evaluation

CIE						**ESE**	**Total**
ST1	**ST2**	**ST3**	**TA1 5**	**TA2 5**	**Attendance 10**		
30			**20**			**50**	**100**

LAB Course Code: CECVL0353	Course Name: Embedded Computing Principles Lab	L	T	P	C
Course Offered in: B. Tech. Fourth Semester EE (VLSI)		**0**	**0**	**4**	**2**

Pre-requisite: Basic of Digital System and Assembly Language Programming

Course Objectives:

This course develops practical skills in programming and interfacing microprocessors and microcontrollers for computational and embedded system applications. It enables students to implement timer/counter functions, interface peripheral devices, and develop assembly-level programs using 8085, 8086, 8051, and ARM architectures.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Apply the knowledge of 8085, 8086 Microprocessor for writing assembly level language.	K3
CO2	Implement timer in 8051 microcontrollers for generating waveforms.	K3
CO3	Analyze the interfacing of various I/O devices with programming.	K4
CO4	Apply the knowledge of ARM Instruction Set to write the program for given application	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	-	3	-	-	-	-	-	2	2	3	3
CO2	3	3	2	-	3	-	-	-	-	-	2	2	3	3
CO3	3	2	2	-	3	-	-	-	-	-	2	3	3	3
CO4	3	2	3	-	3	-	-	-	-	-	2	3	3	3

List Of Practical's (Indicative & Not Limited To)

S. No.	Name of Experiments/ Programs	CO
1	To study architecture of microprocessor 8085.	**CO1**
2	Write a program using 8085 Microprocessor for Hexadecimal addition of two 8-bit Numbers.	**CO1**
3	Write a program using 8085 Microprocessor for Hexadecimal subtraction of two 8-bit Numbers	**CO1**
4	Write a program using 8085 Microprocessor for Hexadecimal addition/subtraction of two 16-bit Numbers	**CO1**
5	Write a program using 8086 Microprocessor for Hexadecimal addition of two 8-bit Numbers.	**CO1**
6	Write a program using 8086 Microprocessor for Hexadecimal subtraction of two 8-bit Numbers.	**CO2**
7	Write a program using 8086 Microprocessor for Hexadecimal addition/subtraction of two 16-bit Numbers.	**CO2**
8	Write a program of flashing LED connected to port 1 of the 8051 Microcontroller.	**CO2**
9	Write a program to generate 10 kHz square wave using 8051 Microcontroller.	**CO2**
10	Write a program to generate a Ramp waveform of 1 KHz using DAC with 8051 micro controllers.	**CO2**
11	To Install AVR Studio.	**CO3**
12	Write an AVR assembly language program to perform the Addition of numbers various data formats.	**CO3**
13	Introduction of the ARM Microntroller Board Lpc 2148.	**CO3**

14	Write a C Program to print “Hello World”.	**CO3**
15	Write a C Program to store data in Accumulator.	**CO3**
16	To install Arduino IDE	**CO4**
17	Interfacing Light Emitting Diode.	**CO4**
18	Interfacing Temperature Sensor (LM35) and/or humidity sensor (e.g. DHT11).	**CO4**
19	Measure the Distance Using Ultrasonic Sensor and Make Led Blink Using Arduino.	**CO4**
20	To install Raspberry Pi.	**CO4**
		Total Hours: 30 hrs.

LAB Course Code: CECVL0351	LAB Course Name: Analog Digital Signal Processing and Communication Lab	L	T	P	C
Course Offered in: B. Tech. EE (VLSI)		**0**	**0**	**4**	**2**

Pre-requisite: Basic understanding of Signal and systems, and communication system.

Course Objectives:

This course provides hands-on experience in signal generation, analysis, and processing using time-domain and frequency-domain techniques. It develops the ability to implement and evaluate analog and digital modulation/demodulation schemes and analyze the performance of digital communication systems under different operating conditions.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Analyze and generate continuous-time and discrete-time signals and perform basic signal operations.	K4
CO2	Apply Fourier Transform techniques, convolution methods, and digital filter design concepts for signal processing applications.	K3
CO3	Demonstration of analog modulation and demodulation techniques such as AM and FM.	K2
CO4	Demonstration of digital modulation and demodulation techniques including ASK, FSK, PSK, and DPSK.	K2
CO5	Develop and analyze front-end digital communication systems using BPSK modulation and demodulation techniques.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	1	1	3	-	-	-	-	-	2	3	2	1
CO2	3	3	3	2	3	-	-	-	-	-	2	3	3	2
CO3	3	2	2	1	3	-	-	-	-	-	2	2	2	1
CO4	3	3	3	2	3	-	-	-	-	-	2	3	3	2
CO5	3	3	3	2	3	-	-	-	-	-	2	3	3	3

List Of Practical's (Indicative & Not Limited To)

S. No.	Name of Experiments/ Programs	CO
1	Write a program to plot the following continuous time and discrete time signals. a) Step Function b) Impulse Function c) Exponential Function d) Ramp Function e) Sine Function f) Cosine Function g) Sinc Function	**CO1**
2	Write a program to perform amplitude-scaling, time-scaling and time-shifting on a given signal	**CO1**
3	Write a program to obtain linear convolution of the given sequences	**CO1**
4	Verify Linear convolution of two sequences using FFT.	**CO2**
5	Verify Circular Convolution of two sequences using FFT	**CO2**
6	Evaluate 4-point DFT of and IDFT of a given sequence.	**CO2**

7	Implement IIR Butterworth analog Low Pass for a given cut off frequency.	**CO3**
8	Using Hamming and Blackman Window Technique with M=5, Design a linear phase LPF with the following desired frequency response $$H_d(e^{j\omega}) = \begin{cases} e^{-j3\omega}, & \omega_{c1} \le \lvert\omega\rvert \le \omega_{c2} \\ 0, & \lvert\omega\rvert \le \omega_{c1} \end{cases}$$	**CO3**
9	To study amplitude modulation and demodulation techniques.	**CO4**
10	To study frequency modulation and determine its modulation factor	**CO4**
11	Study of amplitude shift keying modulator and demodulator	**CO5**
12	Study of frequency shift keying modulator and demodulator.	**CO5**
13	Study of phase shift keying modulator and demodulator.	**CO5**
14	To simulate differential phase shift keying technique using MATLAB software	**CO5**
15	Design a front end BPSK modulator and demodulator.	**CO5**
		Total Hours: 30 hrs.

LAB Course Code: CECVL0352	**Course Name: CMOS Digital Integrated Circuit Lab**	**L**	**T**	**P**	**C**
Course Offered in: B. Tech. Fourth Semester EE (VLSI)		**0**	**0**	**2**	**1**

Pre-requisite: Basis knowledge of MOSFET and Digital Electronics

Course Objectives:

This course provides hands-on experience in the simulation and analysis of MOS devices, CMOS inverters, and digital logic circuits using VLSI design tools. It develops the ability to design, verify, and evaluate CMOS circuits and memory cells while analyzing their performance, power, stability, and reliability characteristics.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Simulate and analyze ID–VGS and ID–VDS characteristics of NMOS and PMOS transistors and extract device parameters	K3
CO2	Analyze the voltage transfer characteristics (VTC) of NMOS and CMOS inverters and determine key parameters such as VOH, VOL, VIH, VIL, and Vth.	K4
CO3	Design and simulate CMOS logic circuits including NOR gates, half adder, and full adder, and verify their truth tables.	K5
CO4	Design and evaluate advanced CMOS circuits such as pass transistor logic, transmission gates.	K5
CO5	Simulate and analyze 6T SRAM cell for functionality and Performance	K4

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	-	3	-	-	-	-	-	-	3	3	3
CO2	3	2	3	-	3	-	-	-	-	-	-	2	3	2
CO3	3	3	2	-	3	-	-	-	-	-	-	3	3	2
CO4	3	1	2	-	3	-	-	-	-	-	-	2	3	3
CO5	3	3	3	-	3	-	-	-	-	-	-	2	3	3

List Of Practical's (Indicative & Not Limited To)

S. No.	**Name of Experiments/ Programs**	**CO**
1	Introduction of Cadence tool/Micro wind, Schematic Editor, Layout Editor.	**CO1**
2	Simulation and Analysis of I_D-V_{GS} and I_D-V_{DS} characteristics of NMOS and PMOS transistors	**CO1**
3	To obtain the NMOSFET parameters: kn, vto, vt, γ.	**CO1**
4	To analyse the voltage transfer characteristics (VTC) of resistive-load NMOS inverter and calculate VOH, VOL, VIH, VIL and Vth.	**CO2**
5	To analyse the voltage transfer characteristics (VTC) of CMOS inverter.	**CO2**
6	To obtain the CMOS Inverter parameters: VOH, VOL, VIH, VIL and Vth.	**CO2**
7	To simulate the CMOS 2 input NOR gates and verify the truth tables	**CO3**
8	To simulate the CMOS 2 input NOR gates and verify the truth tables	**CO3**

9	To simulate the CMOS Half Adder Circuit and verify the truth tables	**CO3**
10	To simulate the CMOS full Adder Circuit and verify the truth tables	**CO3**
11	Design and simulation of a Pass Transistor.	**CO4**
12	Design and simulation of Transmission Gate logic.	**CO5**
13	To design and simulate a 6-transistor SRAM cell**.**	**CO5**
		Total Hours: 15 hrs.

LAB Course Code: CEC0355	LAB Course Name: Verilog-HDL	L	T	P	C
Course Offered in: B. Tech. Fourth Semester EE (VLSI)		**0**	**0**	**6**	**3**

Pre-requisite: Digital System Design

Course Objectives:

This course develops the ability to model, design, and simulate digital circuits and systems using Verilog HDL at different levels of abstraction. It provides hands-on experience in RTL design, switch-level modeling, test bench development, and functional verification of digital systems using simulation tools.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Develop and identify the suitable abstraction level for a particular digital design.	K4
CO2	Develop Verilog codes in gate, dataflow (RTL) modelling levels of abstraction.	K4
CO3	Develop Verilog codes in behavioural (RTL) modelling levels of abstraction	K5
CO4	Design and verify the functionality of digital circuit/system using test benches	K4
CO5	Design and simulate basic Units using switch level modelling.	K4

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	-	3	-	-	-	-	2	2	2	3	2
CO2	3	3	2	-	3	-	-	-	-	2	2	2	3	2
CO3	3	2	2	-	3	-	-	-	-	2	2	2	3	2
CO4	3	2	2	-	3	-	-	-	-	2	2	2	3	2
CO5	3	3	3	-	3	-	-	-	-	2	2	2	3	2

Course Contents/Syllabus		
Unit-1	Evolution of CAD, emergence of HDLs, typical HDL-flow, trends in HDLs, Verilog vs VHDL, Verilog coding vs Software Programming. Top-down and bottom-up design methodology, differences between Units and Unit instances, parts of a simulation, design block, stimulus block. Lexical conventions, data types: value set, registers, vectors, arrays, strings, system tasks, compiler directives. Unit definition, port declaration, connecting ports, hierarchical name referencing.	9 Hour
Unit-2	Modeling using basic Verilog gate primitives, description of and/or and buf/not type gates, rise, fall and turn-off delays, min, max, and typical delays. Continuous assignments, delay specification, expressions, operators, operands, operator types.	9 Hour
Unit-3	Structured procedures, initial and always, blocking and non-blocking statements, delay control, generate statement, event control, conditional statements, Multiway branching, loops, sequential and parallel blocks.	9 Hour
Unit-4	Timing and Delays, Switch-Level Modeling, Logic Synthesis with Verilog HDL, Specify block and Timing checks, Verification and Writing test benches, Timing Analysis of Logic circuits, Downloading of Verilog code in FPGA and CPLD.	9 Hour

Unit-5	Concept of switch level abstraction, MOS Transistor as Switch, Modeling NMOS and PMOS transistors as switches in Verilog, Switch ON/OFF conditions and control signals, Verilog Switch-Level Primitives, Understanding Verilog switch primitives: NMOS, PMOS, Syntax and usage of switch primitives in Verilog code.	9 Hour
		Total Hours: 45 hrs.

List Of Practical's (Indicative & Not Limited To)		
S. No.	**Name of Experiments/ Programs**	**CO**
1	Simulate and synthesize following logic gates using gate level modeling a) AND Gate b) OR Gate c) NOT Gate d) EX-OR Gate e) NAND Gate f) NOR Gate	**CO1**
2	Simulate and synthesize following combinational circuits using gate level modeling a) Half adder b) Full adder c) Half Subtractor d) Full Subtractor e) 4:1 Multiplexer f) 4:2 Encoder g) 1:4 De-multiplexer h) 2:4 Decoder **i)** 1 Bit Comparator 2*2 Bit Multiplier	**CO2**
3	a) Simulate and synthesize binary to gray code converter using gate level modeling. b) Simulate and synthesize gray to binary code converter using gate level modeling.	**CO 2**
4	Simulate and synthesize following combinational circuits using data flow modeling a) Half adder b) Full adder c) Half Subtractor d) Full Subtractor e) 4:1 Multiplexer f) 4:2 Encoder g) 1:4 De-multiplexer h) 2:4 Decoder **i)** 1 Bit Comparator **j)** 2*2 Bit Multiplier	**CO 2**
5	Simulate and synthesize 4-bit parallel adder/Subtractor using data flow modeling.	**CO 2**

<table>
<tr><td>6</td><td>Simulate and synthesize following ALU operations using data flow modeling
<table>
<tr><th>OPCODE</th><th>ALU Operation</th></tr>
<tr><td>1.</td><td>A+B</td></tr>
<tr><td>2.</td><td>A-B</td></tr>
<tr><td>3.</td><td>A Complement</td></tr>
<tr><td>4.</td><td>A*B</td></tr>
</table></td><td>CO2</td></tr>
<tr><td>7</td><td>a) Simulate and synthesize binary to gray code converter using data flow modeling.
b) Simulate and synthesize gray to binary code converter using data flow modeling.</td><td>CO2</td></tr>
<tr><td>8</td><td>Simulate and synthesize following flip flops using behavioral modeling
SR Flip Flop
JK Flip Flop
D Flip Flop
T Flip Flop</td><td>CO3</td></tr>
<tr><td>9</td><td>Simulate and synthesize flip flops using behavioral modeling
a) Using positive edge and negative edge.
b) Using synchronous and asynchronous reset</td><td>CO3</td></tr>
<tr><td>10</td><td>Simulate and synthesize following shift registers using behavioral modeling
a) Serial input serial output
b) Serial input parallel output
c) Parallel input serial output
d) Parallel input parallel output</td><td>CO3</td></tr>
<tr><td>11</td><td>Simulate and synthesize following universal shift register using behavioral modeling</td><td>CO3</td></tr>
<tr><td>12</td><td>Simulate and synthesize following counters using behavioral modeling
a) 2 Bit Counter
b) Mod 5 Counter
c) Decade Counter
d) Ring Counter
e) Johnson Counter</td><td>CO3</td></tr>
<tr><td>13</td><td>Simulate and synthesize array multiplier using behavioral modeling</td><td>CO3</td></tr>
<tr><td>14</td><td>Simulate and synthesize 4:1 MUX by using 2:1 MUX
a) Using a wire
b) Using a reg</td><td>CO3</td></tr>
<tr><td>15</td><td>Simulate and synthesize Moore sequence
a) 1010
b) 1011</td><td>CO3</td></tr>
<tr><td>16</td><td>Simulate and synthesize Mealy sequence
a) 1010
b) 1011</td><td>CO3</td></tr>
</table>

17	Implementation of logic gates on an FPGA and verify gates functionality.	**CO 4**
18	Implementation of 4:1 multiplexer on a FPGA	**CO 4**
19	Implementation of 2*2 multiplier on a FPGA	**CO 4**
20	Implementation of D flip flop on a FPGA	**CO 4**
21	Design and simulation of CMOS inverter using switch level modeling	**CO 5**
22	Simulate and synthesize following logic gates using switch level modeling a) AND Gate b) OR Gate c) NOT Gate d) EX-OR Gate e) NAND Gate f) NOR Gate	**CO 5**
Required Software and Tools (Any one) ISE Simulator (Xilinx) / Xilinx Vivado • AMD-Xilinx-Vivado • Verilog-XL (Cadence) • VCS (Synopsys)		
	Total hours	**35**

Course Code: CNC0301	Course Name: Artificial Intelligence and Cyber Ethics	L	T	P	C
Course Offered in: All Branches		2	0	0	-
Pre-requisite: Basic understanding of AI, Cybercrime, Computer System and Ethics					
Course Objectives:					
The course aims to foster critical thinking about ethical issues, promote responsible use of technology, and ensure students can identify, analyze, and address ethical dilemmas in Artificial Intelligence and cyber domains.					

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Learn key principles of AI ethics, summarizing ethical considerations and applications in AI development and deployment.	**K2**
CO2	Apply policies and framework for Fairness in AI and Machine Learning.	**K3**
CO3	Apply privacy and security concepts, risk management and regulatory compliance in the field of AI and Cyber Security.	**K3**
CO4	Understand the nature of cybercrimes, the principles of intellectual property rights (IPR), and the legal measures necessary to address and prevent these issues.	**K2**
CO5	Describe the impact of AI in Society, employment and workforce.	**K2**

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	-	-	-	-	-	-	-	-	-	-	-	-	-	2
CO2	-	-	-	-	-	-	-	-	-	-	-	-	-	2
CO3	-	-	-	-	-	-	-	-	-	-	-	-	-	3
CO4	-	-	-	-	-	-	-	-	-	-	-	-	-	3
CO5	-	-	-	-	-	-	-	-	-	-	-	-	-	2

Course Contents / Syllabus

Unit 1	**An Overview to AI Ethics**	**5 hours**
Definition of AI Ethical principles in AI, Sources of AI data, Legal implications of AI Security Breaches, Privacy and AI Regulations, Key Principles of Responsible AI, Transparency and Accountability, Dual-Use Dilemma, Human-Centric Design, Introduction to Cyber Laws and Ethics, Historical Development of Cyber laws, Legal frameworks.		
Unit 2	**Fairness and Favoritism in Machine Learning**	**6 hours**
Introduction to Fairness and Bias in AI, Types of Fairness and Bias, Impact of Bias and Fairness in AI, Techniques for Measuring Fairness and Bias, Techniques for Mitigating Bias, Current Policies and Frameworks for Fairness in AI, Bias in Data Collection, Fairness in Data Processing, Generative AI, Types of Bias in Generative AI.		
Unit 3	**AI Ethics and Cybersecurity Principles**	**5 hours**
Importance of Privacy and Security in AI, AI specific Security Tools and Software, Privacy-Preserving Machine Learning (PPML) and Privacy-Preserving Data Mining (PPDM), Risk Management: Risk Assessment and Incident Response, Regulatory Compliance: GDPR, HIPAA, Case Studies: Implementation of AI Ethics guidelines and best practices in engineering projects		
Unit 4	**Cybercrimes, IPR and Legal Measures**	**8 hours**

<table>
<tr><td colspan="6">Types of Cybercrimes and their Impact, Legal measures for Cybercrime Prevention and Prosecution, IPR: Copyrights, Trademarks, Patents, and Trade Secrets, Ethical Implications of Intellectual Property, Cyber Security and Privacy Issues, Cyber Crime Investigations and Digital Evidence Handling, Overview of Indian Cyber Laws (IT Act 2000 and Amendments), Comparative Overview: Indian vs Global Cyber Laws, Case Study: The ATM Heist – Cosmos Bank Cyber Attack (India, 2018).</td></tr>
<tr><td colspan="2">Unit 5</td><td colspan="3">AI Contribution to Social Evolution</td><td>6 hours</td></tr>
<tr><td colspan="6">Positive and Negative Political impacts of AI, Role of AI in social media and Communication Platforms, AI-Generated Content and Deepfakes, Key Technical Stakeholders in AI Deployment: Developers, Researchers, Policymakers, Technical Impacts on Employment and Workforce Automation Technologies: Robotic Process Automation (RPA), Autonomous Systems.</td></tr>
<tr><td colspan="5" align="right">Total Lecture Hours</td><td>30 hours</td></tr>
<tr><td colspan="6">Textbook:</td></tr>
<tr><td colspan="3"></td><td colspan="3">Authors Name</td></tr>
<tr><td colspan="3">1. Artificial Intelligence: A Guide for Thinking Humans</td><td colspan="3">Melanie Mitchell</td></tr>
<tr><td colspan="3">2. Cyber Ethics: Morality and Law in Cyberspace</td><td colspan="3">Richard Spinello, Jones & Bartlett Learning</td></tr>
<tr><td colspan="6">Reference Books:</td></tr>
<tr><td colspan="3"></td><td colspan="3">Authors Name</td></tr>
<tr><td colspan="3">1. Artificial Intelligence and Ethics</td><td colspan="3">S. B. Kishor, Debajit Biswas.</td></tr>
<tr><td colspan="3">2. Cyber Security and Cyber Laws Cengage</td><td colspan="3">Alfred Basta, Nadine Basta, Sattwik Panda</td></tr>
<tr><td colspan="4">Self-Study Content Links:</td><td colspan="2">Duration (in Hrs)</td></tr>
<tr><td>MOOCs</td><td colspan="3"></td><td colspan="2"></td></tr>
<tr><td>Video Lectures</td><td colspan="3">Unit 1: https://www.youtube.com/watch?v=VqFqWIqOB1g
Unit 2: https://www.youtube.com/watch?v=hVJqHgqF59A
Unit 3: https://www.youtube.com/watch?v=O5RX_T4Tg24
Unit 4: https://www.youtube.com/watch?v=RJZ0pxcZsSQ
Unit 5: https://www.youtube.com/watch?v=I9FOswjTSGg</td><td colspan="2">00Hrs 06Min
00Hrs 05Min
00Hrs 01Min
00Hrs 05Min
00Hrs 10Min</td></tr>
<tr><td>Web References</td><td colspan="3"></td><td colspan="2"></td></tr>
</table>

Course Code: CASCC0401	Course Name: Employability Skill Development - II	L	T	P	C
Course Offered in: B. Tech ECE / EE (VLSI)		2	0	0	2

Pre-requisite: Basic Reasoning and Basic Programming Skill

Course Objectives:

Section-A: Develop proficiency in C++ programming, data management, and project development by applying concepts, teamwork, and problem-solving to build practical applications.

Section-B: Enhance quantitative aptitude skills through business mathematics concepts, enabling accurate problem-solving in financial calculations, ratios, and real-world numerical applications.

	Course Outcome: After completion of the course, the student will be able to	**Bloom's Level**
CO1	Apply C++ programming concepts, file handling, and STL techniques to develop efficient programs for data storage and manipulation.	**K3**
CO2	Design and implement a C++ -based project by applying planning, teamwork, and problem-solving skills.	**K6**
CO3	Solve real-life business math problems involving percentages, profit and loss, discounts, interest average calculations and using appropriate mathematical methods	**K3**
CO4	Solve real-life business math problems involving averages, mixtures, and ratios using appropriate mathematical methods	**K3**

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	-	2	3	1	-	3	2	2	2			
CO2	3	3	3	3	3	2	1	3	2	2	2			
CO3	3	3	2	1	-	-	-	1	2	2	2			
CO4	-	-	-	-	1	2	-	3	2	2	-			

Course Contents / Syllabus

Section-A

Unit 1:	**Foundations of C++ Programming and Data Management Techniques**	**8 hours**

Core Fundamentals of C++, Functions & Program Structure, Arrays & Strings, **File Handling:** File streams (ifstream, ofstream, fstream), Reading/writing text files , Saving user data (scores, records, logs) **STL Basics:** vector, array, map, unordered_map set Algorithms (sort, find)

Unit 2	**Project/Game Development**	**8 hours**

Project Planning & Development (Teams, roles, idea pitching and Implement in C++), Mini Project, Project Demonstration and Review

Section-B

Unit 3	**Business Math I**	**8 hours**

Percentage, Profit and Loss, Discount, Simple Interest and Compound Interest, Average

Unit 4	**Business Math II**	**6 hours**

Ratio & Proportion, Partnership, Mixture & Allegation, Clock , Calendar

Total Lectures: 30 hours

Reference Books:		
S. No	**Book Title**	**Author**
1.	A Project-Based Introduction to Programming	Access Point Publishing
2.	Programming: Principles and Practice Using C++	Bjarne Stroustrup
3.	Effective Modern C++	Scott Meyers
4.	Quantitative Aptitude	R S Aggarwal
5.	Verbal & Non-Verbal Reasoning	R S Aggarwal

Mode of Evaluation

CIE							**ESE**	**Total**
ST1	**ST2**	**ST3**	**TA1 10**	**TA2 10**	**TA3 10**	**Attendance 10**		
60			**40**					**100**

Course Code: CAS0403	Course Name: Advanced Engineering Mathematics	L	T	P	C
Course Offered in: B. Tech- ECE / EE (VLSI)		**3**	**1**	**0**	**4**

Pre-requisite: Engineering Math I

Course Objectives:

The objective of this course is to familiarize the students with concepts of statistical techniques, complex variables and Fourier Transform. It aims to show case the students with standard concepts and tools from B. Tech to deal with advanced level of mathematics and applications that would be essential for their disciplines.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Apply the concept of skewness and Kurtosis in the relevant application area.	K3
CO2	Apply the concept of Random Variable and Probability Distributions in real world problems.	K3
CO3	Apply the working methods of complex functions for finding analytic functions.	K3
CO4	Apply the concepts of complex functions for finding Taylor's series, Laurent's series and evaluation of definite integrals.	K3
CO5	Apply the concept of Fourier Transform to solve engineering problems.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	3	1	1	-	1	2	2	2	2	1	-
CO2	3	2	2	3	1	1	-	1	2	2	2	2	1	-
CO3	3	2	1	2	-	-	-	-	1	1	1	2	1	-
CO4	3	2	2	3	-	-	-	-	2	1	1	2	1	-
CO5	3	2	2	3	1	-	-	-	2	1	1	2	1	-

Course Contents / Syllabus

Unit 1	**Statistical Techniques-I**	**9 hours**
Introduction: Measures of central tendency: Mean, Median, Mode, Standard deviation, Quartile deviation, Moments, Skewness, Kurtosis.		
Unit 2	**Random Variables and distribution**	**9 hours**
Random Variable: Definition of a Random Variable, Discrete Random Variable, Continuous Random Variable, Expected Value of a Random Variable, Mean, Variance, Moment Generating Function, Binomial, Poisson, Normal distribution.		
Unit 3	**Complex Variable - Differentiation**	**9 hours**
Limit, Continuity and differentiability, Functions of complex variable, Analytic functions, Cauchy- Riemann equations (Cartesian and Polar form), Harmonic function, Method to find Analytic functions.		
Unit 4	**Complex Variable -Integration**	**9 hours**
Complex integrals, Contour integrals, Cauchy-Goursat theorem (Statement), Cauchy integral formula (Statement), Taylor's series, Laurent's series, Liouvilles's theorem (Statement), Singularities, Classification of Singularities, zeros of analytic functions, Residues, Methods of finding residues, Cauchy Residue theorem (Statement).		
Unit 5	**Integral Transforms**	**9 hours**
Complex Fourier transform, Inverse Transforms, Convolution Theorems, Fourier sine and cosine transform.		

<table>
<tr><td colspan="3" align="right">Total Lecture Hours</td><td>45 hours</td></tr>
<tr><td colspan="4">Textbook:
1. Textbook of Engineering Mathematics- IV, Bali, N.P.
2. Advanced engineering mathematics, Jain, R.K.
3. Higher engineering mathematics, Grewal, B.S.
4. Statistical methods, Gupta, S.P.
5. Advanced engineering mathematics, ZILL, DENNIS G.</td></tr>
<tr><td colspan="4">Reference Books:
1. Introduction to Probability Models, Ross, Sheldon M
2. Probability, Random Variables and Stochastic Processes, Papoulis, Athanasios
3. Advanced engineering mathematics, Kreyszig, E.</td></tr>
<tr><td colspan="2">Self-Study Content Links:</td><td colspan="2">Duration (in Hrs)</td></tr>
<tr><td>MOOCs</td><td>1. https://www.coursera.org/learn/complex-analysis

2. https://www.coursera.org/learn/introductiontoprobability

3. https://www.futureskillsprime.in/course/probability-and-statistics/</td><td colspan="2">10 Hrs
7 Hrs
30 Hrs</td></tr>
<tr><td>Video Lectures</td><td>https://youtu.be/xhAdXdkx4IY?si=qmeWymorZjTRP5Gb
https://youtu.be/D-ugYU-5KD0?si=5GnIImQh0KZkhdng
https://youtu.be/Am7Bu4aytEQ?si=tPOufctBkK0fa-41
https://youtu.be/KQkOxZSZpZw?si=HWag4HVOEnAYFEea
https://youtu.be/TL7yAkOA9D0?si=Zpde-JLws0Du9UT4</td><td colspan="2">27 Min
28 Min
28 Min
27 Min
29 Min</td></tr>
<tr><td>Web References</td><td>https://ocw.mit.edu/courses/18-04-complex-variables-with-applications-spring-2018/pages/syllabus/</td><td colspan="2">3 hrs</td></tr>
</table>

\

Course Code: CECVL0401	Course Name: Low Power VLSI Design	L	T	P	C
Course Offered in: B.Tech. EE (VLSI)		**2**	**0**	**0**	**2**

Pre-requisite: Basic knowledge of Digital Electronics, CMOS circuits, MOSFET operation, and VLSI Design fundamentals.

Course Objectives:

This course introduces the principles of power dissipation and energy-efficient design in digital integrated circuits. It develops the ability to analyze and design low-power arithmetic and memory architectures using techniques that optimize power, performance, and area in VLSI systems.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Demonstrate the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability.	K3
CO2	Illustrate the different low-power design approaches and optimization of switched capacitance.	K3
CO3	Discuss the different low-power high speed adders.	K2
CO4	Apply the concepts of low voltage and low power to different multipliers.	K3
CO5	Apply the concepts of low voltage and low power to different memories.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	-	-	-	-	-	-	-	-	2	3	2
CO2	3	2	2	-	-	-	-	-	-	-	-	2	3	2
CO3	3	2	2	-	-	-	-	-	-	-	-	2	3	2
CO4	3	2	2	-	-	-	-	-	-	-	-	2	3	2
CO5	3	2	2	-	-	-	-	-	-	-	-	2	3	2

Course Contents / Syllabus

Unit 1	**Fundamentals of Low Power VLSI Design**	**6 hours**

Need for Low Power Circuit Design, Sources of Power Dissipation, Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation-Reverse diode leakage current, Sub threshold leakage current, Glitching Power Dissipation.

Unit 2	**Low Voltage Process Technology**	**6 hours**

Low-Power Design through Voltage Scaling: VTCMOS circuits, MTCMOS circuits, Architectural Level Approach —Pipelining and Parallel Processing Approaches.

Estimation and Optimization of Switching Activity: The Concept of Switching Activity, Reduction of Switching Activity, Reduction of Switched Capacitance-System Level Measures, Circuit Level Measures, and Mask level Measures.

Unit 3	**Low-Voltage Low-Power Adders**	**6 hours**

Introduction, Standard Adder Cells, CMOS Adder's Architectures for Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Carry Skip Adders.

Unit 4	**Low-Voltage Low-Power Multipliers**	**6 hours**

Overview of Multiplication, Booth Multiplier-Booth’s algorithm, modified Booth algorithm, Introduction to Tree Multiplier (Wallace and Dada multipliers) and 4:2 Compressors.		
Unit 5	**Low Power Random Access Memory Circuits**	**6 hours**
Sources of power dissipation in SRAMs, Low power SRAM circuit techniques, Sources of power dissipation in DRAMs, Low power DRAM circuit techniques.		
	Total Lecture Hours	**30 hours**

Textbook:	
	Authors Name
1. CMOS Digital Integrated Circuits -Analysis and Design	Sung-Mo Kang, Yusuf Leblebici
2. Low-Voltage, Low-Power VLSI Subsystems	Kiat-Seng Yeo, Kaushik Roy
Reference Books:	
	Authors Name
1. Principles of CMOS VLSI Design	Neil H. E. Weste and K. Eshraghian
2. Low Power VLSI CMOS Circuit Design	Bellamour, and M. I. Elmasri
3. Low Power Digital CMOS Design	Anantha P. Chandrakasan and Robert W. Brodersen
4. Low-Power CMOS VLSI Design	Kaushik Roy and Sharat C. Prasad

Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	1.https://www.youtube.com/watch?v=C8kiblD2riw&list=PL1wj50dotxPPsCrF16rHnkfID1TP2LJ5Z. 2.https://www.youtube.com/watch?v=0ykJeTGqv6M&list=PLB3F0FC99B5D89571&index=27 3.https://www.youtube.com/watch?v=K2kL7pMnL_0&list=PLVDb88QIgXkeeUo6I2oudLvc76GbLGrTi 4. https://www.youtube.com/watch?v=ORtlxpW_LMU&t=10s 5. https://www.youtube.com/watch?v=EMcW9EggY0s 6.https://www.youtube.com/watch?v=jK6xr4r06tU&list=PLB3F0FC99B5D89571&index=16	00Hrs 52Min 00Hrs 54Min 00Hrs 12Min 00Hrs 36Min 01Hrs 35Min 01Hrs 56Min
Web References		

Course Code: CEC0401	Course Name: CMOS Analog Integrated Circuit	L	T	P	C
Course Offered in: B. Tech. ECE and EE (VLSI)		**3**	**0**	**0**	**3**

Pre-requisite: Basic understanding of electronic devices, circuit theory, and operational amplifiers.

Course Objectives:

This course introduces the operation and modeling of MOSFET devices and develops the ability to analyze and design CMOS analog circuits, including amplifiers, differential pairs, current mirrors, and biasing networks. It also provides an understanding of frequency response, bandwidth, and stability considerations in analog integrated circuit design.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Explain the operation of MOSFETs, including small-signal modeling and short-channel effects.	K2
CO2	Design and evaluate single-stage CMOS amplifiers considering gain, impedance, and operating region constraints.	K4
CO3	Analyze differential amplifier configurations for differential gain, common-mode response, and active load operation.	K4
CO4	Design CMOS current mirrors and biasing networks for stable current generation and analog circuit operation.	K3
CO5	Analyze frequency response and stability-related trade-offs in CMOS analog amplifiers using pole-zero and bandwidth concepts.	K4

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	3	-	-	-	-	-	-	-	-	2	3	2
CO2	3	2	3	-	-	-	-	-	-	-	-	2	3	2
CO3	3	3	3	-	-	-	-	-	-	-	-	2	3	2
CO4	3	3	3	-	-	-	-	-	-	-	-	2	3	2
CO5	3	3	3	-	-	-	-	-	-	-	-	2	3	2

Course Contents / Syllabus

Unit 1	**Basic MOS Device Physics**	**10 hours**
General Considerations: MOSFET as a Switch, MOSFET Structure, MOS Symbols, MOS I/V Characteristics, Threshold Voltage, Derivation of I/V Characteristics, MOS Transconductance, Second-Order Effects, MOS Device Models, MOS Device Layout, MOS Device Capacitances, MOS Small-Signal Model.		
Unit 2	**Single-Stage Amplifiers**	**9 hours**
Analytical justification of operating region suitable for amplification/switching, Design of CS amplifier with different loads, Limitations of diode connected load, Improving output impedance of CS amplifier through feedback, Source Follower, Common-Gate, Cascode Stage, Folded Cascode.		
Unit 3	**Differential Amplifiers**	**8 hours**
Single-Ended and Differential Operation, Basic Differential Pair, Qualitative Analysis, Quantitative Analysis, Degenerated Differential Pair, Common-Mode Response, Differential Pair with MOS Loads		
Unit 4	**Current Mirrors and Biasing Techniques**	**9 hours**

Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors, Large-Signal Analysis, Small-Signal Analysis, Common-Mode Properties, Other Properties of Five-Transistor OTA, Biasing Techniques, CS Biasing, CG Biasing, Source Follower, Differential Pair Biasing		
Unit 5	**Frequency Response of Amplifiers**	**9 hours**
General Considerations, Miller Effect, Association of Poles with Nodes, Common-Source Stage, Source Followers, Common-Gate Stage, Cascode Stage, Differential Pair, Differential Pair with Passive Loads, Differential Pair with Active Load, Gain-Bandwidth Trade-Offs, One-Pole Circuits, Multi-Pole Circuits		
	Total Lecture Hours	**45 hours**

Textbook:	
	Authors Name
1. Design of Analog CMOS Integrated Circuit	Behzad Razavi
2. Analog Integrated Circuit Design	David A. Johns, Ken Martin

Reference Books:	
	Authors Name
1. CMOS analog circuit design	Allen, Phillip E., and Douglas R. Holberg
2. VLSI Design Techniques for Analog and Digital Circuits	Geiger, Allen and Stradder

Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	1.https://www.youtube.com/watch?v=dlOlxAcfBo4&list=PLunAuxHqEAijgoKKoo7aYYvXtjiVwbin5&index=1 2.https://www.youtube.com/watch?v=0OH9d72ZX7s&list=PLunAuxHqEAijgoKKoo7aYYvXtjiVwbin5&index=2 3.https://www.youtube.com/watch?v=GmhFnm6mdxY&list=PLunAuxHqEAijgoKKoo7aYYvXtjiVwbin5&index=3 4.https://www.youtube.com/watch?v=jfizMWm3Q0I&list=PLunAuxHqEAijgoKKoo7aYYvXtjiVwbin5&index=4 5.https://www.youtube.com/watch?v=UTo4IGXxzlk&list=PLunAuxHqEAijgoKKoo7aYYvXtjiVwbin5&index=7 6.https://www.youtube.com/watch?v=RgpH9_sy5iI&list=PL_b8tSqlo138huGY9amrru2EA28Zcxgyy&index=6 7. https://www.youtube.com/watch?v=PxsY1U8aMso&t=1982s 8.https://www.youtube.com/watch?v=XbM1WgGXQc&list=PLZvoNERCg2SxxSN-gBoW7bR_UGQmLj7Fx	01Hrs 04Min 01Hrs 02Min 00Hrs 59Min 01Hrs 04Min 01Hrs 05Min 00Hrs 48Min 00Hrs 48Min 00Hrs 47Min
Web References		

Course Code: CECVL0402	Course Name: Product Architecture Models and Firmware	L	T	P	C
Course Offered in: B.Tech. EE(VLSI)		**3**	**0**	**0**	**3**

Pre-requisite: Microcontroller basics and Programming basics

Course Objectives:

This course introduces the architecture, instruction set architecture (ISA), and programming model of RISC-V processors. It develops the ability to design, implement, and debug RISC-V firmware while providing a strong foundation in processor programming concepts applicable to modern embedded and computing systems.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Illustrate the benefits of RISC V microarchitecture IP.	K2
CO2	Relate RISC V ISA with other conventional controllers ISA.	K2
CO3	Infer supervisor and machine mode programming of RISC V.	K2
CO4	Design and debug RISC V firmware.	K6
CO5	Develop RISC V based Embedded system configuration.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	2	-	-	-	-	-	-	-	2	2	1
CO2	3	3	2	2	-	-	-	-	-	-	-	3	3	2
CO3	3	3	3	2	-	-	-	-	-	-	-	3	3	2
CO4	3	3	3	2	-	-	-	-	-	-	-	3	3	2
CO5	3	3	3	3	-	-	-	-	-	-	-	3	3	2

Course Contents / Syllabus

Unit 1	**Fundamentals of Product Architecture**	**10 hours**

SoC overview, MCUs of SoC, Architecture models, CISC Processor Architecture, CISC Instruction Set Architecture, RISC Architecture, RISC Instruction Set Architecture, CISC vs RISC an insight, Instruction Pipeline in RISC, ARM Architecture: A case Study in RISC, Trends in RISC Processor Development, RISC -V Open-Source Architecture and Ecosystem, RISC-V Impact on Semiconductor Industry.

Unit 2	**RISC V ISA**	**9 hours**

Introduction to RISC V ISA, Base user-level ISA, Base programmers' model, Instruction length encoding, Instruction formats, Load & Store, Integer computational instructions, Memory model, System instructions, Extensions: Compression instructions, Floating point instructions, Packed SIMD.

Unit 3	**Designing and Building Custom Firmware for the Future**	**9 hours**

Open-Source Firmware, Open-Source System Firmware Development, Open-Source Device Firmware Development, Open-Source Manageability Firmware Development, Build Tools, Configuration and Flashing Tools, Source Control Management Overview, Coding Standards.

Unit 4	**System Firmware Insights: Debugging Challenges and Future Innovations**	**8 hours**

<table>
<tr><td colspan="4">Hardware-Assisted Debugging - Generic Debugging, SoC-Specific Debugging, OxM-Specific Debugging, Software-Assisted Debugging, Core Security Design, LITE Firmware Development, Feature Kernel Design, Multithreaded Firmware Design, Hardware Innovation.</td></tr>
<tr><td>Unit 5</td><td colspan="2">Embedded Linux System Design and Development</td><td>9 hours</td></tr>
<tr><td colspan="4">Architecture of Embedded Linux, Kernel Architecture, User Space, Communication between Kernal and user space, Linux Start-Up Sequence, GNU Cross-Platform Toolchain, Configuration and building process, System debugging and Profiling. Introduction Board Support Package, Memory Map and Interrupt Management, Introduction to PCI Subsystem, Introduction RTOS.</td></tr>
<tr><td colspan="3">Total Lecture Hours</td><td>45 hours</td></tr>
<tr><td colspan="4">Textbook:</td></tr>
<tr><td colspan="2"></td><td colspan="2">Authors Name</td></tr>
<tr><td colspan="2">1. Firmware Development – A Guide to Specialized Systemic Knowledge</td><td colspan="2">Subrata Banik, Vincent Zimmer</td></tr>
<tr><td colspan="2">2. Embedded Linux System Design and Development</td><td colspan="2">P. Raghavan, Amol Lad, Sriram Neelakandan Boca Raton</td></tr>
<tr><td colspan="4">Reference Books:</td></tr>
<tr><td colspan="2"></td><td colspan="2">Authors Name</td></tr>
<tr><td colspan="2">1. The RISC-V Instruction Set Manual Volume I: Base User-Level ISA</td><td colspan="2">Andrew Waterman.</td></tr>
<tr><td colspan="3">Self-Study Content Links:</td><td>Duration (in Hrs)</td></tr>
<tr><td>MOOCs</td><td colspan="2"></td><td></td></tr>
<tr><td>Video Lectures</td><td colspan="2">1.https://youtube.com/playlist?list=PLuv3GM6gsE01L9yDO0e5UhQapkCPGnY3&si=OHZf4gSCZarUpYp8
2.https://youtube.com/playlist?list=PL3_RRtJ5Iqgg94er7ErGAUSyhTXwPv6zy&si=Y83Kc64uHf4LUf4
3. https://youtu.be/Uep3yWaVxqc?si=CNXNQ4uHbk5yR24k
4.https://youtube.com/playlist?list=PLM3lhmHjSeIRa3jW7nrKA0c2UpjsJeaHl&si=4SU4ZY_KPEi-ub18
5.https://youtube.com/playlist?list=PLUQpHm_JtukJ5tUmlcWKpcVbGfYy0MfxI&si=Nk9sLHiz-s0PA4k4</td><td>00Hrs 44Min
01Hrs 48Min
00Hrs 07Min
02Hrs 27Min
04Hrs 30Min</td></tr>
<tr><td>Web References</td><td colspan="2"></td><td></td></tr>
</table>

Course Code: CEC0411	Course Name: Data Analytics	L	T	P	C
Course Offered in: B. Tech ECE / EE(VLSI)		3	0	0	3

Pre-requisite: Basic Programming, Basics of digital electronics

Course Objectives:

This course introduces the fundamental concepts and methodologies of data analytics and develops the ability to preprocess, analyze, and interpret data from diverse sources. It equips students with skills in exploratory data analysis and data visualization to extract meaningful insights and support data-driven decision-making.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Describe the fundamental concepts of data analytics in the areas that plays major role within the realm of data science.	K2
CO2	Explain and exemplify the most common forms of data and its representations.	K2
CO3	Apply data pre-processing techniques on heterogeneous datasets.	K3
CO4	Analyze data using exploratory data analysis.	K4
CO5	Apply visualization tool to analyze and draw inference from different types of data sets w.r.t different application scenarios.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	-	3	-	-	-	-	-	2	2	2	2
CO2	3	2	2	-	3	-	-	-	-	-	2	2	3	2
CO3	3	3	2	-	3	-	-	-	-	-	2	3	3	2
CO4	3	3	3	-	3	-	-	-	-	-	2	2	3	2
CO5	3	3	3	-	3	-	-	-	-	-	2	2	2	2

Course Contents / Syllabus

Unit 1	Foundations of Data Science: Concepts, Tools, and Applications	10 hours

Introduction to Data Science, Evolution of Data Science, Skillsets needed, Lifecycle, Need for Data Science, Datafication, Types of Data Analysis, Data Science Tools and technologies, Analysis Vs Analytics Vs Reporting, Applications of Data Science in various fields, Use cases of Data science-Facebook, Netflix, Amazon, Uber, AirBnB.

Unit 2	Data Types and Statistical Foundations	09 hours

Types of Data: structured, semi-structured, unstructured data, Numeric, Categorical, Graphical, High Dimensional Data, Transactional Data, Spatial Data, Social Network Data, standard datasets, Sources of Data, Data manipulation in various formats, for example, CSV file import and export data in R/Python. Measure of central tendency (Mean, Median, Mode), Central limit theorem, Skewness, Variance, SD, Covariance, Correlation, Normal distribution, Margin of Error.

Unit 3	Data Preprocessing and Visualization	10 hours

Form of Data Pre-processing, data Attribute and its types, KDD process, Inconsistent Data, Data Cleaning: Missing Values, Noisy Data, Discretization and Concept hierarchy generation (Binning, Clustering, Histogram),

Data Integration and Transformation. Data Reduction: Data Cube, Data Compression, Numerosity Reduction, R-Square, Adjusted R-Square, Significance of p-value.		
Unit 4	**Data Cleaning, Transformation, and Exploration**	**08 hours**
Variable Selection, Removing Redundant variables, identifying outliers, Removing Outliers, Time series Analysis, Data transformation and dimensionality reduction techniques such as Principal Component Analysis (PCA), Factor Analysis (FA) and Linear Discriminant Analysis (LDA), Univariate and Multivariate Exploratory Data Analysis. Data Wrangling using R/Python.		
Unit 5	**Data Visualization with Tableau**	**08 hours**
Introduction to Tableau, Installation and configuration of Tableau. Creating Your First visualization: Getting started with Tableau Software, Using Data file formats, connecting your Data to Tableau, creating basic charts using the Show me panel. Tableau Calculations: Overview of SUM, AVR, and Aggregate Features, Creating custom calculations and fields, Manipulating Data in Tableau: Cleaning-up the data with the Data Interpreter, structuring your data, Sorting, and filtering Tableau data, Pivoting Tableau data. Advanced Visualization Tools: Using Filters, Using the Detail panel, Using the Size panels, customizing filters, Using and Customizing tooltips, formatting your data with colors, Creating Dashboards & Stories, Distributing & Publishing Your Visualization.		
	Total Lecture Hours	**45 hours**

Textbook:	
	Authors Name
1. Data Analysis and Data Mining	John Wiley & Sons
2. Making sense of Data: A practical Guide to Exploratory Data Analysis and Data Mining	Glenn J. Myatt.
Reference Books:	
	Authors Name
1. The Data Science Handbook, Field Cady	John Wiley & Sons
2. Data Mining Concepts and Techniques	Jiawei Han, Micheline Kamber, Jian Pei, Morgan Kaufmann

Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	1.https://www.youtube.com/playlist?list=PLEiEAq2VkUUKgEFXH1tBbHwq38oWYDScU 2.https://www.youtube.com/watch?v=dcXqhMqhZUo 3. https://www.youtube.com/watch?v=VaSjiJMrq24 4. https://www.youtube.com/watch?v=tDu_KIlXaB0 5. https://www.youtube.com/watch?v=ZX8vmcSTCrc 6. https://www.youtube.com/watch?v=I3450sh1eDo	00Hrs 54Min 00Hrs 06Min 29Hrs 13Min 00Hrs 05Min 00Hrs 54Min 01Hrs 56Min
Web References		

Course Code: CEC0412	Course Name: Sensor Technology	L	T	P	C
Course Offered in: B. Tech ECE		**3**	**0**	**0**	**3**

Pre-requisite: Knowledge of basic semiconductor devices and principle

Course Objectives:

To provide students with the fundamental concepts of smart sensors and IoT technologies, enabling them to understand sensor principles, industrial sensing applications, and IoT device architectures. The course also aims to develop the ability to apply IoT-based solutions for real-world societal and industrial challenges.

Course Outcome: After completion of the course, the student will be able to		**Bloom's level**
CO1	Explain various real time products using smart sensors.	K2
CO2	Use the sensors for measurement of displacement, force, and pressure.	K3
CO3	Employ and analyze commonly used sensors in industry for measurement of temperature, position, accelerometer, vibration sensor, and level.	K4
CO4	Explain the key elements of an IoT device.	K2
CO5	Analyze challenges, and issues related to IoT and apply IoT on social society problems.	K4

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	-	-	-	-	-	-	-	2	2	2	2
CO2	3	3	2	-	-	-	-	-	-	-	2	3	3	2
CO3	3	3	2	-	-	-	-	-	-	-	2	3	3	2
CO4	3	2	2	-	-	-	-	-	-	-	2	3	3	2
CO5	3	3	2	-	-	-	-	-	-	-	2	3	3	2

Course Contents / Syllabus

Unit 1	**Sensors & Transducers**	**`9 hours**

Sensors, Actuators & Transducers: Definition, Classification of sensors, Measurement of displacement using Potentiometer, LVDT & Optical Encoder, Measurement of force using strain gauge, Measurement of pressure using LVDT-based diaphragm & piezoelectric sensor, Introduction to sensors most widely used in computer and mobile phones: Temperature, Pressure, Humidity, Toxic Gas, pH sensor, sound sensor, magnetic field sensor, Motion (Infra-red) sensor, barometer, and Gyroscope.

Unit 2	**Measurement of physical parameters**	**9 hours**

Measurement of temperature using Thermistors, Thermocouple & RTD, Concept of thermal imaging, Measurement of position using Hall effect sensors, Proximity sensors: Inductive & Capacitive, Use of proximity sensor as accelerometer and vibration sensor, Working Principles of Flow Sensors: Ultrasonic & Laser, Level Sensors: Ultrasonic & Capacitive.

Unit 3	**Hardware and Advanced Sensors**	**9 hours**

RFID Principles and components, Intelligent Sensors: General Structure of smart sensors & its components, Characteristic of smart sensors: Self calibration, Self-testing & self-communicating, Selection of Sensors for Practical Applications, Application of smart sensors: Automatic robot control & automobile engine control.

Unit 4	**Introduction to IoT and its basic fundamentals**	**9 hours**
Basics of Computer Networking and its Topologies, OSI Model, TCP/IP Protocol Introduction to IoT and its Characteristics, IoT Architectures and its Physical & Logical Design, Enabling Technologies in IoT, M2M Communication, Suite.		
Unit 5	**IoT Development Boards and Use Cases**	**9 hours**
IoT Development Boards: Arduino IDE and Board Types, Arduino IDE coding, Libraries, Raspberry Pi, Node MCU, Communication Technologies: Zigbee, BLE, Use Cases: Smart Cities, Home Automation, Smart Street Light, Smart Hospitals		
	Total Lecture Hours	**45 hours**

Textbook:	
	Authors Nam
1. Sensors Handbook	Sabrie Soloman.
2. Sensors and Instrumentation	A.K. Sawhney
3. The Internet of Things	Michael Miller
Reference Books:	
	Authors Name
1. Raspberry Pi Cookbook	Simon Monk
2. Arduino Cookbook: Recipes to Begin, Expand, and Enhance Your Projects	Brian Jepson, Michael Margolis, Nicholas Robert Weldin
3. Intelligent Technologies for Sensors-Applications, Design, and Optimization for a Smart World	S. Kannadhasan, R. Nagarajan, Alagar Karthick.

Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	1. https://www.arduino.cc/en/software. 2. https://www.raspberrypi.com/ 3. https://nptel.ac.in/courses/108108147 4. https://www.youtube.com/watch?v=wn1UCt9Z6NQ&t=56s 5. https://www.youtube.com/watch?v=GfaHdjApnhU.	00Hrs 09Min 00Hrs 05Min 00Hrs 07Min
Web References		

LAB Course Code: CECVL0451	LAB Course Name: Low Power VLSI Design Lab	L	T	P	C
Course Offered in: B-Tech ECE / EE (VLSI)		0	0	4	2

Pre-requisite: CMOS circuit operation and power dissipations

Course Objectives:

To provide students with practical knowledge of low-power VLSI design by analyzing power dissipation mechanisms and optimizing combinational and sequential CMOS circuits for energy efficiency. The course also aims to develop proficiency in implementing leakage reduction techniques and synthesizing low-power RTL architectures using industry-standard design methodologies and simulation tools.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Analyze and measure static, dynamic, and short-circuit power dissipation components in CMOS logic circuits using electronic simulation tools.	K3
CO2	Design and optimize combinational and sequential logic blocks for minimal Power-Delay Product (PDP) using alternative logic styles.	K4
CO3	Implement and evaluate leakage reduction methodologies including MTCMOS, power gating, and transistor stacking configuration.	K3
CO4	Synthesize and validate low-power RTL-level architectures using clock-gating, multi-voltage domains, and energy-efficient multiplier algorithms.	K4

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	2	3	-	-	-	-	-	2	2	3	2
CO2	3	3	2	2	3	-	-	-	-	-	2	2	3	2
CO3	3	3	2	2	3	-	-	-	-	-	2	2	3	2
CO4	3	3	2	2	3	-	-	-	-	-	2	2	3	2

List Of Practical's (Indicative & Not Limited To)	CO
1. Analyze CMOS inverter power characteristics using Voltage Transfer Characteristics (VTC) and evaluate short-circuit, static, and dynamic power dissipation mechanisms.	**CO1**
2. Design 2-input NAND and NOR gates using Static CMOS and Pass Transistor Logic (PTL), and compute and compare their Power Delay Product (PDP) performance.	**CO1**
3. Implement a 1-bit Full Adder using Conventional CMOS, Transmission Gate (TG), and compare total power consumption.	**CO1**
4. Design D Flip-Flop and JK Flip-Flop circuits and analyze energy consumption under varying clock frequencies.	**CO2**
5. Simulate a 6T SRAM bit cell and implement techniques for reducing write-driver power consumption.	**CO2**
6. To design an adiabatic logic inverter circuit.	**CO2**
7. To design CMOS logic circuits using Low-Vt and High-Vt transistors.	**CO3**

8. Implement PMOS header or NMOS footer sleep transistors and measure leakage reduction during sleep mode.	**CO3**
9. To apply forward and reverse body bias voltages to MOS transistors and study their effects on threshold voltage variation and leakage current reduction in CMOS circuits.	**CO3**
10. To design and implement clock gating logic in a synchronous register circuit and evaluate the reduction in dynamic power consumption using simulation and power analysis tools.	**CO4**
11. To design a conventional array multiplier. And to implement bypass or row-switching techniques for low-power operation.	**CO4**
12. To implement Dynamic Voltage Scaling (DVS) techniques in CMOS circuits and study the effect of supply voltage variation on circuit delay, power consumption, and overall energy efficiency.	**CO4**
	Total: 30 Hrs

LAB Course Code: CEC0451	LAB Course Name: CMOS Analog Integrated Circuit Lab	L	T	P	C
Course Offered in: B.Tech. ECE / EE (VLSI)		0	0	2	1

Pre-requisite: Basic understanding of electronic devices, circuit theory, and operational amplifiers. Familiarity with SPICE simulation and mathematical tools like differential equations is also recommended.

Course Objectives:

To provide students with practical knowledge of CMOS analog circuit design by analyzing MOSFET characteristics, amplifier configurations, and current mirror circuits. The course also aims to develop proficiency in designing, simulating, and laying out CMOS circuits while evaluating their frequency response and performance using industry-standard EDA tools.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Analyze MOSFET characteristics and extract design parameters.	K3
CO2	Design and simulate CMOS amplifier stages (CS, CG, Cascode).	K3
CO3	Implement and evaluate differential amplifiers and current mirrors.	K4
CO4	Analyze the frequency response of amplifier circuits and interpret results.	K4
CO5	Design, simulate, and layout of CMOS inverter.	K3

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	2	-	3	-	-	-	-	-	2	3	2	2
CO2	3	2	3	-	3	-	-	-	-	-	2	3	2	2
CO3	3	3	3	-	3	-	-	-	-	-	2	3	3	3
CO4	3	3	3	-	3	-	-	-	-	-	2	3	3	3
CO5	3	3	2	-	3	-	-	-	-	-	2	3	3	3

List Of Practical's (Indicative & Not Limited To)	**CO**
1. Study of NMOS characteristics using DC and transient analysis; extraction of Vth and Region of operation.	**CO1**
2. Extraction of MOSFET design parameters (gm, ro) using gm/ID methodology.	**CO1**
3. Design and Simulation of Single Stage Common Source Amplifiers with resistive load evaluation of gain and biasing.	**CO1**
4. Design and Simulation of Single Stage Common Source Amplifiers with diode connected load.	**CO2**
5. Design and Simulation of Single Stage Common Gate Amplifiers analysis of input impedance and bandwidth.	**CO2**
6. Design and Simulation of Single Stage Cascode Common Source Amplifiers evaluation of gain enhancement and output resistance.	**CO2**
7. Design and Simulation of a Differential Amplifier with active load, Analysis of differential gain and CMRR.	**CO3**
8. Design and Simulation of Basic Current Mirror.	**CO3**

9. Design and Simulation of Cascode Current Mirror, analysis of output resistance and improved current stability.	**CO3**
10Design of Two Stage CMOS Op-Amp Circuit.	**CO4**
11. Analysis of Frequency response of various amplifiers (Common Source, Cascode, Differential Amplifier).	**CO4**
12. Pre Layout Simulation of CMOS inverter.	**CO4**
Total Hours: 15 hrs.	

Course Code: CECVL0455	Course Name: VLSI Principles, RTL Design And Verification (Workshop II)	L	T	P	C
Course Offered in: B-Tech EE (VLSI)		0	0	6	3

Pre-requisite: Digital System Design

Course Objectives:

To provide students with practical knowledge of the VLSI design flow and RTL design using Verilog HDL for modeling, simulation, synthesis, and implementation of digital systems. The course also aims to develop proficiency in applying appropriate coding methodologies, programming constructs, and EDA tools to design optimized and synthesizable hardware.

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Explain the fundamentals of VLSI design flow, RTL design concepts, and their significance in modern digital systems.	K2
CO2	Apply Verilog HDL constructs for modeling, simulation, and implementation of combinational and sequential digital circuits.	K3
CO3	Analyze and utilize top-down and bottom-up design methodologies along with EDA tools for efficient RTL design and development.	K4
CO4	Develop skills in functional verification using testbenches and verification techniques.	K4
CO5	Explain the RTL synthesis process, optimization techniques, and transformation from RTL description to gate-level implementation.	K2

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	2	2	-	3	-	-	-	-	-	3	3	3	2
CO2	3	2	2	2	3	-	-	-	-	-	3	3	3	3
CO3	3	2	2	2	3	-	-	-	-	-	3	3	3	2
CO4	3	2	3	2	3	-	-	-	-	-	3	3	3	2
CO5	3	2	3	2	3	-	-	-	-	-	3	3	3	2

Course Contents / Syllabus

Unit 1	**RTL Design and Verilog Fundamentals**	**9 hours**

Introduction to Logic Design and Evolution, System and Logic Design Abstractions, Integrated Circuit Design and Methodologies: RTL Design, Functional Verification, Synthesis, Physical Design, Introduction of Verilog HDL, Verilog Design Description: Structural, Behavioral, and Synthesizable RTL Designs, Key Verilog Terminologies: Arithmetic, Logical, and Relational Operators.

Unit 2	**System Design Implementation**	**9 hours**

Logic Design without Memory elements, RTL Guidelines for Logic Design without Memory elements, Logic Design with Memory elements, RTL Guidelines for Logic Design with Memory elements, Complex design using Verilog RTL, Situation Driven Hardware Design, Data Path and Controller-Part 1&2, Modeling Memory & Register Banks, Basic Pipeline Concepts, Pipeline Modeling, Pipeline Implementation-Part 1&2, Verilog

Modeling of Processor, Design & Implement Micro Architecture from Vendor Specification. Simulation Using Verilog, Introduction to PLD, FPGA as Programmable ASIC, SRAM Based FPGA, FPGA Design Flow, Logic Realization Using FPGA, Design Guidelines for FPGA-Based Designs.		
Unit 3	**RTL Verification Standards**	**9 hours**
Verification Guidelines: Introduction to Verification, The Verification Process, The Verification Plan, The Verification Methodology Manual, Basic Testbench Functionality, Directed Testing, Methodology Basics, Constrained-Random Stimulus, Functional Coverage Introduction to Data Types: Built-in Data Types, Fixed-Size Arrays, Dynamic Arrays, Queues, Associative Arrays, Linked Lists, Array Methods, choosing a Storage Type, Creating New Types with typedef, User-Defined Structures, Enumerated Types, Constants, Strings, Expression Width, and Net Types.		
Unit 4	**Testbench Design and OOP Concepts**	**9 hours**
Procedural Statements and Routines: Introduction, Procedural Statements, Tasks, Functions, and Void Functions, Routine Arguments, Returning from a Routine, Local Data Storage, Time Values **Basic Object-Oriented Programming (OOP):** Introduction to OOP in System Verilog, Creating Classes, OOP Terminology, Creating New Objects, Object Deallocation, Using Objects and Static Variables vs. Global Variables, Class Routines and Defining Routines Outside of the Class, Scoping Rules, Using One Class Inside Another and Understanding Dynamic Objects, Copying Objects, Public vs. Private, Building a Testbench **Connecting the Testbench and Design**: Introduction to Interface Constructs, Separating Testbench and Design Logic, The Interface Construct, Stimulus Timing, Interface Driving and Sampling, Connecting It All Together and Top-Level Scope, Program – Unit Interactions, System Verilog Assertions and The Four-Port ATM Router.		
Unit 5	**Advanced System Design and Verification**	**9 hours**
Threads and Interprocess Communication (IPC): Introduction to Threads and IPC and Working with Threads, Interprocess Communication Mechanisms and Events, Semaphores and Mailboxes, Building a Testbench with Threads, and IPC **Advanced Object-Oriented Programming (OOP):** Introduction to Advanced OOP Concepts and Inheritance, Factory Patterns, Type Casting and Virtual Methods, Composition, Inheritance, and Alternatives, Copying Objects and Callbacks. **Functional Coverage Strategies:** Introduction to Functional Coverage and Coverage Types, Functional Coverage Strategies and Simple Functional Coverage Example, Anatomy of a Cover Group and Triggering a Cover Group, Data Sampling, Cross Coverage and Coverage Options, Parameterized Cover Groups and Analyzing Coverage Data, Measuring Coverage Statistics During Simulation Advanced Interfaces: Introduction to Advanced Interfaces with Virtual Interfaces with the ATM Router, Connecting to Multiple Design Configurations, Procedural Code in Interfaces.		
	Total Lecture Hours	**45 hours**
Textbook: 1. Verilog HDL: A Guide to Digital Design and Synthesis, Samir Palnitkar 2. Writing Testbenches Using System Verilog, Janick Bergeron		
Reference Books: 1. System Verilog for Verification: A Guide to Learning the Testbench Language Features, Chris Spear and Greg Tumbush.		

2. System Verilog and Verification Tutorials by ASIC World.		
Self-Study Content Links:		**Duration (in Hrs)**
MOOCs		
Video Lectures	1. https://www.youtube.com/watch?v=OrM8B8ENvMU 2. https://www.youtube.com/watch?v=AfVG-va5TSE 3. https://www.youtube.com/watch?v=FE7QoJ6udac 4. https://www.youtube.com/watch?v=uTpPSY_0fi4 5. http://digimat.in/nptel/courses/video/108106191/L30.html	**30 hours**
Web References		

LAB Course Code: CCSCC0452	LAB Course Name: Problem Solving Approaches	L	T	P	C
Course Offered in: B. Tech. ECE / EE (VLSI)		0	0	2	1

Pre-requisite: Programming Language C/C++ or Java or Python

Course Objectives:

Problem-solving in computer programming involves a structured approach to identifying, analyzing, and resolving coding challenges. The process typically includes thoroughly understanding the problem, decomposing it into smaller, manageable parts, designing an appropriate algorithm, implementing the solution through code, and performing testing and debugging to ensure correctness and efficiency

Course Outcome: After completion of the course, the student will be able to		**Bloom's Level**
CO1	Develop logic-based solutions using control statements, recursion and bit manipulation to solve basic and intermediate computational problems	K6
CO2	Implement and manipulate arrays and strings using fundamental and advanced searching sorting techniques	K3
CO3	Analyze and debug code for logical errors and improve the efficiency of the solution using appropriate data structures and algorithmic Pattern	K4

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2	PSO3
CO1	3	3	3	2	2	1	2	2	-	-	2	3	3	2
CO2	3	3	2	2	2	-	2	-	-	-	2	2	2	2
CO3	3	3	2	2	3	1	2	2	-	-	3	3	3	2

List Of Practical's (Indicative & Not Limited To)

Problem Statements need to be discussed in lab session: Control Statements	**CO**

1. Secure Password Generator

A company wants to create a secure password generator for their employees. The password must be based on specific numeric properties to enhance its complexity and security. Write a program to validate and generate a secure password according to the following rules:

1. Prime Number Validation:

- The user must input a 3-digit number. The program should first check if the number is a prime number.
- If it is not a prime number, the user should be prompted to enter another number until a valid prime number is provided.

2. Sum of Digits Check:

- Once a valid prime number is entered, calculate the sum of its digits. If the sum of the digits is not divisible by 3, ask the user to enter another prime number until a valid one is found.

3. Armstrong Number Check:

- Check entered prime number is Armstrong or not? If Armstrong are found, prompt the user to enter another prime number and repeat the process.

Password Generation:

Concatenate the 1 if entered prime number is Armstrong otherwise 2 with the sum of the digits of the valid prime number to form the secure password.

Example Scenario:

Sample Input

Enter a 3-digit prime number: 153 Sum of
digits of 153 = 9

The sum is divisible by 3. 153 is Armstrong number ***Sample***
Output

Secure Password: 19

2. Write a function to input electricity unit charges and calculate total electricity bill according to the given condition: For first 50 units Rs. 0.50/unit for next 100 units Rs. 0.75/unit For next 100 units Rs. 1.20/unit For unit above 250 Rs. 1.50/unit an additional surcharge of 20% is added to the bill

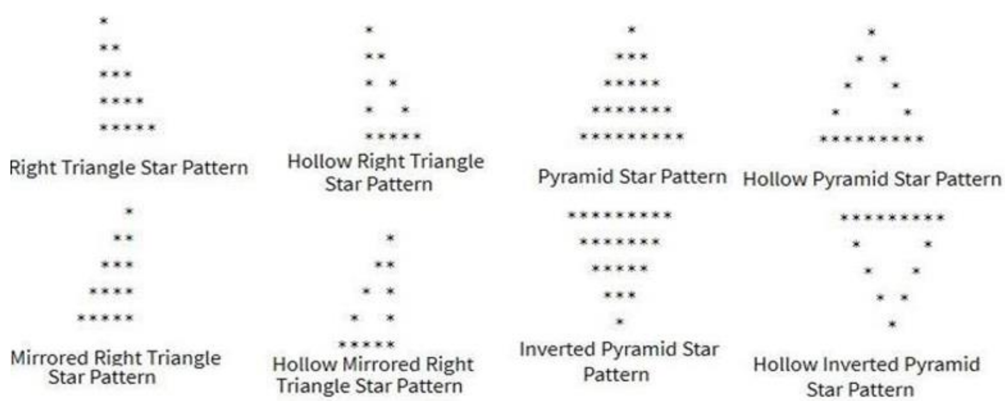
3. Write a method to generate a secure code which the sum of all possible palindrome numbers between given two numbers. For Example:

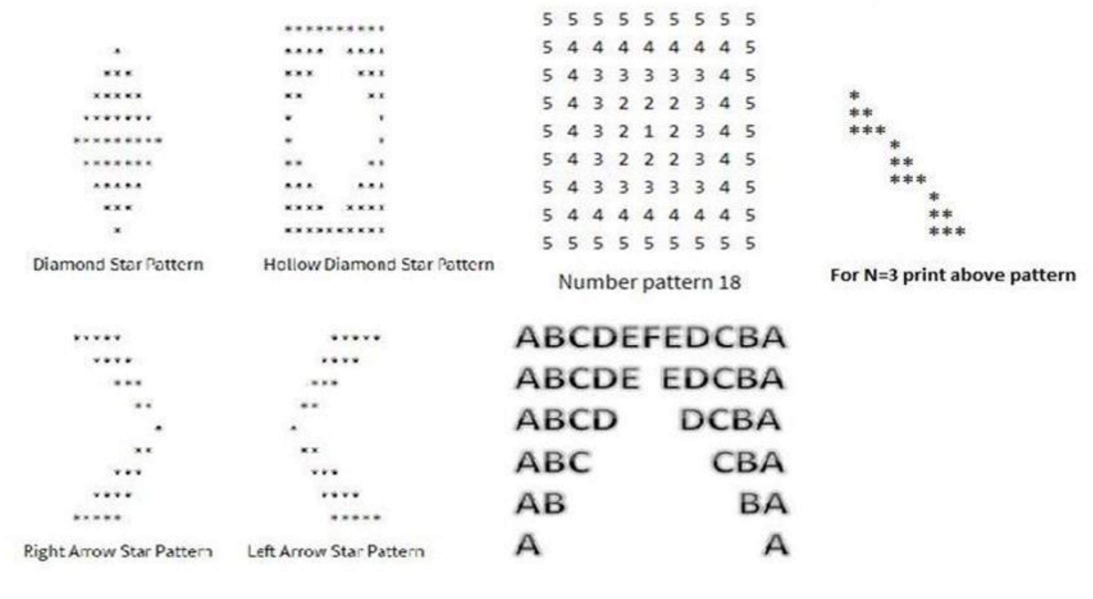
Input: 10, 80

Output: 308

Explanation: All palindrome numbers between 10 & 80 are: 11,22,33,44,55,66,77 Password=
11+22+33+44+55+66+77 = 308

4. Draw **the following Patterns for N=5**





Problem Statements need to be discussed in lab session: Recursive Approach (Basic)

1. Write a program that takes an integer n as input and prints the multiplication table of n from n * 1 to n * 10. The output should clearly show each multiplication step.
2. Write a program to calculate the sum of all integers from 1 to a given number N. The program should take N as input and output the total sum using iteration or recursion.
3. **Find the GCD of Two Numbers Using Recursion:**
   Write a recursive function to calculate the Greatest Common Divisor (GCD) of two numbers using Euclid's algorithm. The function should take two integers as input and return their GCD.
4. **Find the LCM of Two Numbers Using Recursion:**
   a. Write a program to compute the Least Common Multiple (LCM) of two numbers using recursion. You may use the relationship LCM(a, b) = |a * b| / GCD(a, b) and a recursive function for GCD.

Problem Statements need to be discussed in lab session: Bit Manipulation

1. Write a program to count the number of set bits (1s) in the binary representation of a given integer. The program should efficiently use bitwise operations to perform the task without converting the number to a string.
2. Write a program that takes a number and a bit position as input and checks whether the bit at that position is set (1) or clear (0). Use bitwise operators to perform the check
3. Given a number and a position, write a program to toggle (invert) the bit at the given position using bitwise operations. The result should reflect the updated value of the number after flipping the bit
4. Write a program to compute the XOR of all numbers from 1 to n using a mathematical pattern (not a loop). Use bitwise XOR properties to achieve an efficient solution
5. Given an array of size n-1 containing unique elements from 1 to n, find the missing number using bit manipulation (preferably XOR approach) without sorting or using extra space.

6. Given an array where all elements repeat twice except two elements that appear only once, write a program to find the two non-repeating elements using bitwise operations in linear time and constant space.
7. Write a program to check if a given number is a power of two using bit manipulation. A number is a power of two if it has exactly one set bit in its binary representation.
8. Given two integers A and B, write a program to count how many bits need to be flipped to convert A to B. Use XOR to find differing bits and count the number of set bits.
9. Write an efficient program to count the total number of set bits in binary representations of all numbers from 1 to n. Optimize the approach using bitwise logic and recursion.
10. Write a program to calculate the square of a number using only bitwise operations and addition. Do not use multiplication, division, or any power functions.
11. Write a function to add two integers using bitwise operations only. Avoid using the + or - operators. Implement logic using XOR and AND operations for binary addition.
12. Write a program to generate the power set (all subsets) of a given set using bitwise representation. Each subset can be represented by a binary number where each bit indicates inclusion of the corresponding element.
Problem Statements need to be discussed in lab session: Arrays (Try to use sliding window, prefix sum, cadence, recursion, bit manipulation, two pointer approaches)
1. Sarah is assisting the "MathMinds Club" in creating passwords for their online platform. They have a list of numbers, some stable and some unstable. Define a function that can help Sarah calculate the password according to the given scenario. Scenario: • There are N numbers provided. • A number is stable if each digit appears the same number of times. • A number is unstable if the frequency of its digits is not the same. • The password is computed as the sum of all stable numbers minus the sum of all unstable numbers. • Consider only those numbers in the list that have more than equal to three digits. For example: Input: N=5 List: 12, 1313, 122, 678, 898 Output: Password: 971
2. Given an array of integers, including possible negative values, you are allowed to modify at most one element by doubling its value. The goal is to find the maximum possible sum of any subarray after making this modification. **Input**: arr = [-2, 1, -3, 4, -1, 2, 1, -5, 4] Expected Output: • Original Maximum Subarray Sum: 6 (achieved from [4, -1, 2, 1]) Maximum Sum After Modification: 10(achieved from [8, -1, 2, 1], where the value 4 is doubled to 8).
3. For a given string, generate a pattern based on the following rules: **Input:** A string of characters (e.g., "HAT").

Output: Generate patterns by replacing characters with the numeric value 1 and process the patterns as described below:

1. **Replace one character at a time with 1:**
   - For each character in the string, replace it with 1, keeping the other characters unchanged.
   - Example for "HAT":

1AT, H1T, HA1

2. **Replace two characters at a time with 1:**
   - Replace every combination of two characters with 1, keeping the remaining character unchanged.
   - If 1s are consecutive, replace them with their sum (e.g., 11T becomes 2T).
   - Example for "HAT":

11T → 2T, H11 → H2, 1A1

3. **Replace all characters with 1:**
   - Replace all characters in the string with 1.
   - If there are consecutive 1s, sum them up (e.g., 111 becomes 3).
   - Example for "HAT": 111

→ 3

Final Output

For the string "HAT", the output should be: 1AT, H1T, HA1, 2T, H2, 1A1, 3.

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4. Given a sorted array arr [] and a target value, the task is to count triplets (i, j, k) of valid indices, such that arr[i] + arr[j] + arr[k] = target and i < j < k.

Examples:

Input: arr[] = [-3, -1, -1, 0, 1, 2], target = -2

Output: 4

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5. You are given an array prices[] where prices[i] represents the price of a given stock on day i. You want to maximize your profit by choosing a single day to buy one stock and choosing a different day in the future to sell that stock. Write a program to return the maximum profit you can achieve from this transaction. If no profit is possible, return 0.

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6. Find **the "Kth" max and min element of an array:**

Given k, find the k-th smallest and k-th largest element in the array. Input: arr = [7, 10, 4, 3, 20, 15], k = 3

Output: Kth Smallest: 7, Kth Largest: 10

Given k, find the k-th smallest and k-th largest element in the array. Input: arr = [7, 10, 4, 3, 20, 15], k = 3

Output: Kth Smallest: 7, Kth Largest: 10

---

7. Sort a binary array with value 0,1 and 2 using constant space and one pass (Dutch national Flag algorithm)

Input: [0, 2, 1, 2, 0]

Output: [0,0,1,2,2]

---

8. Find **longest consecutive subsequence:**

Return the length of the longest consecutive elements sequence. Input: [1, 9, 3, 10, 4, 20, 2]

Output: 4 (Sequence: 1, 2, 3, 4)

9. Given a number of bits and a number K. In one flip you can toggle exactly K consecutive bits. With only this flip operation available, convert the string into all 1. Input String: 0000110000 and K=3

Following are four flip operations by using which all bits converted into 1's. Flip1-1110110000 Flip2-1110110111

Flip3-1111000111 Flip4- 1111111111

If it is not possible to convert all bits into one's then print "IMPOSSIBLE".

10. Given a list of non-negative integers, arrange them in such a way that they form the largest possible number. Since the result can be very large, return it as a string in **O(N log N)** time complexity.

Example-1	**Example-2**
Input: N = 5 Arr[] = {3, 30, 34, 5, 9} **Output**: 9534330	**Input**: N = 4 Arr[] = {54, 546, 548, 60} **Output**: 6054854654

11. Given an array arr[] of size n containing distinct integers within the range [1, n+2], find the two missing numbers from the first n+2 natural numbers.

Constraints:

- The solution must run in **O(N) time** and use **O(1) extra space**.
- The array does not contain duplicate values.

Examples:

Input: arr[] = [1, 2, 4, 6, 3, 8], n = 6

Output: 5, 7

12. Given a string str of lowercase alphabets and a number k, the task is to print the minimum value of the string after removal of k characters. The value of a string is defined as the sum of squares of the count of each distinct character present in the string. Return the minimum possible required value. **Examples:**

Input: str = "abccc", k = 1

Output: 6

Input: str = "aabcbcbcabcc", k = 3

Output: 27

Expected Time Complexity: O(n+klog(p))

Note: Here n is the length of string and p is number of distinct alphabets and k number of alphabets to be removed

13. Given a non-negative integer **S** represented as a string, remove **K** digits from the number so that the new number is the smallest possible.

Note: The given *num* does not contain any leading zero.

Expected Time Complexity: O(|S|).

	Example 1: Input S=”149811, K=3 Output: 111	Example 2: Input S=”1002991, K=3 Output: 21	

14. You are given a two-dimensional grid board[][] of size n * m consisting of English letters and a string target. Your task is to determine whether the target word can be formed by sequentially connecting letters from the grid. You may move to adjacent cells **horizontally or vertically** (not diagonally), and **a cell may not be reused** once it is part of the current path.

Examples:

Input:

board[][] = [['C', 'A', 'T'], ['R', 'A', 'K'], ['T', 'O', 'N']],

target = "CART" **Output:**

true **Explanation:**

You can trace the word "CART" through the path: C → A → R → T (moving horizontally and vertically, without repeating cells).

15. Given an encoded string **s**, the task is to decode it. The encoding rule is:

- **k[encodedString],** where the **encodedString** inside the square brackets is being repeated exactly **k** times. Note that **k** is guaranteed to be a positive integer, and encoded String contains only lowercase English alphabets.

Note: The test cases are generated so that the length of the output string will never exceed 10^5.

Examples:

Input: s = "1[b]"

Output: "b"

Input: s = "3[b2[ca]]"

Output: "bcacabcacabcaca"

**Competitive coding list will be shared with the students.*

Total Hours: 15 hrs.

CIE						ESE	Total
PS1	**PS2**	**PS3**	**TA1** **5**	**TA2** **5**	**Attendance** **10**		
30			**20**			**50**	**100**

Course Code: CNC0302/CNC0402	Course Name: Environmental Science	L	T	P	C
Course Offered in: CSE/CS/IT/CSE(AI)/CSE(AIML)/CSE(IOT)/CSE(AI)/CSE(DS)/CSE-R/M.Tech (Int) / MCT / CSE (CYS)		2	0	0	NA

Pre-requisite: Basic knowledge of biology, chemistry, ecology, geology, mathematics, and understanding of human impacts on natural systems.

Course Objectives:

To help the students in realizing the inter-relationship between man and environment and help the students in acquiring basic
knowledge about environment.

Course Outcome: After completion of the course, the student will be able to		Bloom's Knowledge Level (KL)
CO1	Understand the basic principles of ecology and the environment. Ecosystem: Basic concepts, components of ecosystems, food chains and food webs. Ecological pyramids	K2
CO2	Understand the different types of natural recourses like food, forest, Minerals and energy and their conservation	K2
CO3	Understand the different types of pollution, pollutants, their sources, effects, and their control methods.	K2
CO4	Understand the basic concepts of sustainable development, Environmental Impact Assessment (EIA) and different acts related to environment	K2

CO-PO Mapping (Scale 1: Low, 2: Medium, 3: High)

CO-PO MAPPING	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PSO1	PSO2
CO1	3	3	2	2	-	3	3	2	2	-	2	2	2
CO2	3	3	2	2	-	3	3	2	2	-	2	2	2
CO3	3	3	2	2	-	3	3	2	2	-	2	2	2
CO4	3	3	2	2	-	3	3	3	2	-	2	2	2

Course Contents / Syllabus

UNIT 1	Basic Principle of Ecology and Biodiversity	5 HOURS

Definition, Scope and basic principles of ecology and environment. Ecosystem: Basic concepts, components of ecosystem. Food chains and food. Webs. Ecological pyramids, Energy flow in ecological systems, Characteristics of different ecosystems. Biogeochemical Cycles: Importance, gaseous and sedimentary cycles. Carbon, Nitrogen, Phosphorus and Sulphur Cycles. Biodiversity and their importance, Threats to biodiversity, major causes, extinction's, vulnerability of species to extinction, IUCN threat categories, Red data book. Strategies for biodiversity conservation, principles of biodiversity conservation in-situ and ex-situ conservation strategies Mega diversity zones and Hot spots, concepts, distribution and importance.

UNIT 2	Natural Resources and Ecological succession	5 HOURS

Natural resources and associated problems. Forest resources: Use and over- exploitation, deforestation. Timber extraction, mining, dams and their effects on forest and tribal people. Mineral resources: Use and exploitation, environmental effects of extracting and using mineral resources. Food resources: World food problems, changes caused by agriculture and over- grazing, effects of modern agriculture, fertilizer-pesticide problems, water logging, and salinity. Land resources: Land as a resource, land degradation, man induced landslides. Equitable use of resources for sustainable lifestyles. Non-Renewable Energy Resources: Fossil fuels and their reserves, Nuclear energy, types, uses and effects, Renewable Energy Resources: hydropower, Solar energy, geothermal, tidal and wind energy, Biomass energy, biogas and its advantages. Ecological succession-Types, stages, examples of ecological succession

UNIT 3	Pollution and Waste Management	5 HOURS

Air pollution: sources of air pollution, Primary and secondary air pollutants. Origin and effects of SOX, NOX, Cox, CFC, Hydrocarbon, control of air pollution. Water pollution: sources and types of water pollution, Effects of water pollution, Eutrophication, Soil pollution: Causes of soil pollution, Effects of soil pollution, Major sources of and effects of noise pollution on health, Radioactive and thermal pollution sources and their effects on surrounding environment. Solid waste disposal and its effects on surrounding environment, Introduction to E- Waste, Types and classification of E- Waste, Impacts of E- Waste on environment and human health,E-Waste management and recycling., Climate change, global warming, acid rain, ozone layer depletion.

UNIT 4	Environmental Assessment and Legislation	5 HOURS

Women education, Role of NGOs regarding environmental protection, Bio indicators and their role, Natural disasters and disasters

management, Aims and objectives of Environmental Impact Assessment (EIA). Salient features of following Acts: Environmental Protection Act, 1986, Wildlife (Protection) Act, 1972.Water (Prevention and control of pollution) Act, 1974. Forest (Conserving) Act, 1980. Definition and concept of sustainability, impacted areas of sustainable development, Global initiative, and issues on sustainable development UN SDGs, System Thinking and Sustainability.	
Total Lecture Hours	**20 HOURS**

Textbook:

S.No	Book Title with publication agency & year	Author
1	Brady, N.C. 1990. The nature and properties of Soils, Tenth Edition. Mac Millan Publishing Co., New York	Brady, N.C
2	Sodhi G.S. 2005, Fundamentals of Environmental Chemistry: Narosa Publishing House, New Delhi.	Sodhi G.S
3	Dash, M.C. (1994), Fundamentals of Ecology, Tata Mc Graw Hill, New Delhi.	Dash, M.C

Reference Books:

1	Rao M.N. and H.V.N. Rao, 1989 : Air Pollution, Tata McGraw Hill Publishing Co. Ltd., New Delhi	Rao M.N. and H.V.N. Rao
2	A Text Book of environmental Science By Shashi Chawla	Shashi Chawla

Self-Study Content Links:

MOOC'S		
VIDEO LECTURES	https://www.youtube.com/watch?v=T21OO0sBBfc https://www.youtube.com/watch?v=qt8AMjKKPDo https://www.youtube.com/watch?v=brF0RWJyx9w https://www.youtube.com/watch?v=GK_vRtHJZu4	**7 min 42 sec** **15 min** **3 min 25 sec** **4 min 25 sec**
WEB REFERENCES	https://www.youtube.com/watch?v=yqev1G2iy20, https://www.youtube.com/watch?v=_74S3z3IO_I, https://www.youtube.com/watch?v=jXVw6M6m2g0	**28 min** **31 min 35 sec** **11 min**