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Printed Page:-3 **Subject Code:- AEC0502**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA
(An Autonomous Institute Affiliated to AKTU, Lucknow)
B.Tech
SEM: V - THEORY EXAMINATION (2025 - 2026)
Subject: CMOS Digital Integrated Circuit

Time: 3 Hours **Max. Marks: 100**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* ***three Sections -A, B, & C.*** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION-A 20

1. Attempt all parts:-

1-a. What does MOSFET stands for? (CO1,K1) 1

(a) Metal Oxide Semiconductor Field Effect Transistor
(b) Modern Oxidized Silicon based Field Effect Transistor
(c) Modern Oxidized Silicon based Force Effect Transistor
(d) Metal Oxide silicon Field Equivalent Transistor

1-b. In which region, MOSFET perform as a switch? (CO1,K1) 1

(a) Cut-off
(b) Linear
(c) Saturation
(d) Option 1& 2

1-c. Pull-down network (PDN) connects output node to _____ . (CO2, K1) 1

(a) VDD
(b) Ground
(c) Input
(d) All of these

1-d. Which of the following CMOS logic circuits will contain parallel NMOS transistors? (CO2,K1) 1

(a) NOR
(b) NAND
(c) NOT
(d) Transmission gate

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1-e. Switch logic is based on _____ . (CO3,K2) 1

(a) Pass transistors
(b) Transmission gates
(c) Pass transistors and Transmission gates
(d) Design rules

1-f. In Pseudo-nMOS logic, n transistor operates in (CO3,K1) 1

(a) Cut-off region
(b) Saturation region
(c) Resistive region
(d) Non saturation region

1-g. In which method regularity is used to reduce complexity? (CO4,K2) 1

(a) random approach
(b) hierarchical approach
(c) algorithmic approach
(d) semi-design approach

1-h. FPGA stands for… (CO4,K1) 1

(a) Field Program Gate Array
(b) First Program Gate Array
(c) Field Programmable Gate Array
(d) First programmable Gate Array

1-i. ASIC cell library is a collection of _____ . (CO5,K2) 1

(a) standard cells with different logic functions
(b) standard cells with different fan-out capabilities
(c) standards cells with different fan-in capabilities
(d) all of the above

1-j. Input and output pads are made up of _____ . (CO5,K1) 1

(a) polysilicon
(b) metal
(c) silicon
(d) carbon

2. Attempt all parts:-

2.a. Can a MOSFET conduct in both directions? Explain it. (CO1,K2) 2

2.b. Draw the truth table of full adder. (CO2,K2) 2

2.c. What is a Pass transistor? (CO3,K1) 2

2.d. What do you understand by design rules in VLSI? (CO4,K1) 2

2.e. What is floorplanning in ASIC design? (CO5,K1) 2

SECTION-B 30

3. Attempt all parts:-

3.a. Answer any one of the following:-

3.a.(i) Explain the working of a CMOS NAND gate with neat circuit diagram. (CO1,K3) 6

3.a.(ii)	Design XOR gate using CMOS logic circuit. (CO1,K3)	6
3.b. Answer any one of the following:-		
3.b.(i)	Differentiate between combinational and sequential circuit design.(CO2,K2)	6
3.b.(ii)	Explain Successive Approximation Register (SAR). (CO2,K2)	6
3.c. Answer any one of the following:-		
3.c.(i)	Describe NORA CMOS design styles in detail. (CO3,K2)	6
3.c.(ii)	Realize the following Boolean function using Pseudo-NMOS logic:Y = A + B (C + D). (CO3,K3)	6
3.d. Answer any one of the following:-		
3.d.(i)	Explain in detail principle and operation of FPGA. Also write down the applications. (CO4,K2)	6
3.d.(ii)	What is Stick Diagram? What are the uses of Stick diagram? (CO4,K1)	6
3.e. Answer any one of the following:-		
3.e.(i)	Explain in brief the floorplanning and placement in ASIC design. (CO5,K1)	6
3.e.(ii)	Explain Y Chart in VLSI. (CO5,K2).	6

SECTION-C 50

4. Answer any one of the following:-

4-a.	Explain the voltage transfer characteristics curve of CMOS inverter and explain different regions of operation. (CO1,K2)	10
4-b.	Derive the expression for total power dissipation in CMOS inverter. (CO1,K3)	10

5. Answer any one of the following:-

5-a.	Explain the weighted resistor type and R-2R type DAC. (CO2,K2)	10
5-b.	With a neat block diagram, explain the working of two bit flash type analog to digital Converter. (CO2,K2)	10

6. Answer any one of the following:-

6-a.	Compare the different dynamic CMOS logic styles. (CO3,K3)	10
6-b.	What is the charge sharing problem in domino logic? How to resolve this problem? (CO3,K3)	10

7. Answer any one of the following:-

7-a.	Explain in detail the design hierarchy, regularity, modularity and locality in view of VLSI design methodology. (CO4,K1)	10
7-b.	Design a stick diagram for two input NAND and NOR logic gates. (CO4,K3)	10

8. Answer any one of the following:-

8-a.	Explain in detail the steps involved in ASIC design. (CO5,K2)	10
8-b.	Explain the goals and objectives of detailed routing and also explain the routing method used in ASIC physical design. (CO5,K2)	10