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Printed Page:-4 **Subject Code:- BMICSE0305X**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA
(An Autonomous Institute Affiliated to AKTU, Lucknow)
M.Tech Integrated
SEM: III - THEORY EXAMINATION (2025 - 2026)
Subject: Computer Architecture & Parallel Processing

Time: 3 Hours **Max. Marks: 100**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*
1. *This Question paper comprises of* ***three Sections -A, B, & C.*** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*
2. *Maximum marks for each question are indicated on right -hand side of each question.*
3. *Illustrate your answers with neat sketches wherever necessary.*
4. *Assume suitable data if necessary.*
5. *Preferably, write the answers in sequential order.*
6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION-A 20

1. Attempt all parts:-

1-a. Select the fastest memory in computer? (CO1, K2) 1

(a) Register
(b) Cache Memory
(c) Main Memory
(d) Secondary Memory

1-b. The data transfer rate of a bus depends mainly on_____. (CO1, K2) 1

(a) Bus width and clock speed
(b) Addressing mode
(c) Operating system
(d) Cache size

1-c. The multiplier is stored in_____ (CO2, K1) 1

(a) PC Register
(b) Shift Register
(c) Cache
(d) None

1-d. The 'heart' of the processor performing operations is_____ . (CO2, K1) 1

(a) Control Unit
(b) ALU
(c) Memory
(d) Register

1-e. Control hazard occurs due to_____(CO3, K3) 1

(a) Arithmetic intructions
(b) Branch instruction
(c) Load instructions
(d) Store instructions

1-f. The main task of the control unit during execution phase is to_____ (CO3, K2) 1

(a) Fetch data
(b) Activate appropriate control signals
(c) Store data
(d) Load Program

1-g. The main goal of parallel architectures is to_____ (CO4, K2) 1

(a) Increase single-thread performance
(b) Improve power consumption
(c) Execute multiple instructions simultaneously
(d) Simplify programming models

1-h. The most significant advantage of virtual memory is_____ (CO4, K1) 1

(a) Faster CPU speed
(b) Larger apparent memory space
(c) Reduced power consumption
(d) Direct access to disk storage

1-i. Protocol maintaining cache coherence by recording sharers in memory is_____ (CO5, K3) 1

(a) Cache-based directory protocol
(b) Snooping protocol
(c) Token coherence
(d) Memory-based directory protocol

1-j. Main disadvantage of memory-based directory protocol is___ (CO5,K2) 1

(a) Complexity
(b) Slower access time
(c) Not supporting invalidation
(d) High storage overhead proportional to processors

2. Attempt all parts:-

2.a. Describe the use of Register Transfer Language? (CO1, K3) 2

2.b. Discuss the function of a shift register in multiplication hardware? (CO2, K3) 2

2.c. Explain the role of control unit. (CO3, K2) 2

2.d. Describe the responsibilities of cache memory. (CO4, K3) 2

2.e. Define a directory-based cache coherence protocol. (CO5, K1) 2

SECTION-B 30

3. Attempt all parts:-

3.a. Answer any one of the following:-

3.a.(i) Draw and explain a common bus system for 4 registers of 4 bits using multiplexers. 6

(CO1, K3)

3.a.(ii)	Explain general register organization with the help of a diagram. (CO1, K3)	6
3.b. Answer any one of the following:-		
3.b.(i)	Illustrate the design and operation of a 1-bit ALU for both arithmetic and logic operations using its truth table and circuit diagram. (CO2, K3)	6
3.b.(ii)	Describe the hardware implementation of Booth's algorithm for multiplying two numbers. (CO2, K3)	6
3.c. Answer any one of the following:-		
3.c.(i)	Explain the steps involved in the fetch-decode-execute cycle with the help of a neat diagram. (CO3, K3)	6
3.c.(ii)	Discuss the Flynn's classification in detail. (CO3. K2)	6
3.d. Answer any one of the following:-		
3.d.(i)	Discuss the need for parallelism and how it improves the system performance. (CO4, K3)	6
3.d.(ii)	Examine the structure of a write-through and write back cache system. (CO4, K4)	6
3.e. Answer any one of the following:-		
3.e.(i)	Illustrate the role of centralized and distributed directory architectures in maintaining coherence in scalable systems. (CO5, K3)	6
3.e.(ii)	Explain the difference between sequential consistency and relaxed consistency models with suitable examples. (CO5, K3)	6

SECTION-C 50

4. Answer any one of the following:-

4-a.	Discuss the various types of addressing modes with the help of atleast two examples for each. (CO1, K3)	10
4-b.	Describe the push and pop operations of register stack and memory stack and also write the microoperations for each task. (CO1, K3)	10

5. Answer any one of the following:-

5-a.	Describe the steps involved in multiplying binary numbers using a 4 bit array multiplier. Also, explain the role of each components used in the array structure (CO2, K3)	10
5-b.	Represent the given numbers (i) $(-55.17)_{10}$ (ii) $(0.329)_{10}$ using both IEEE 754 single precision and double precision formats. Also, mention the advantages of IEEE 754. (CO2, K4)	10

6. Answer any one of the following:-

6-a.	A system uses a non-pipelined processor with an average instruction execution time of 10 ns. A pipelined processor of the same system uses 5 stages, each with a delay of 2 ns. (i) Calculate the speedup achieved through pipelining. (ii) Evaluate whether the pipeline improves system throughput significantly. Also, explain the importance of pipelining. (CO3, K4)	10
6-b.	Explain the working of micro programmable control unit. (CO3, K3)	10

7. Answer any one of the following:-

7-a.	A system uses 3-page frames for storing process pages in main memory. It uses the	10

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LIFO and optimal page replacement policy. Assume that all the page frames are initially empty. What is the total page faults, total page hits, page fault ratio and page hit ratio that will occur while processing the page reference string given below - 4, 7, 6, 1, 7, 6, 1, 2, 7, 2 ? Also, mention its advantages and disadvantages. (CO4, K4)

7-b. Differentiate between the VI, MSI, MESI, and Dragon protocols. (CO4, K3) 10

8. Answer any one of the following:-

8-a. Discuss in detail the working of Directory-based Coherence Protocols and distinguishing between Memory-based and Cache-based approaches. (CO5, K3) 10

8-b. Explain the architecture of the SGI Origin system. Discuss how NUMA memory organization supports scalability. (CO5, K3) 10