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Printed Page:-3 **Subject Code:- AMTVL0114**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA
(An Autonomous Institute Affiliated to AKTU, Lucknow)
M.Tech
SEM: I - THEORY EXAMINATION (2025 - 2026)
Subject: Microchip Fabrication Technology

Time: 3 Hours **Max. Marks: 70**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* ***three Sections -A, B, & C.*** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION-A 15

1. Attempt all parts:-

1-a. The active components in an IC are (CO1, K1) 1

(a) Transistors & diodes
(b) Capacitors
(c) Registers
(d) None of these

1-b. SiO2 acts as : (CO2, K1) 1

(a) Conductor
(b) Semiconductor
(c) Insulator
(d) None of these

1-c. What is next step after Photolithography? (CO3,K2) 1

(a) Oxidation
(b) Diffusion
(c) Metallization
(d) Orientation

1-d. In the fabrication of NPN transistors in an IC, buried layer on P type substrate is (CO4, K2) 1

(a) P+ doped
(b) N+ doped
(c) used to reduce the parasitic capacitance
(d) located in the emitter region

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1-e.	Deposition rate is given as (CO5,K2) (a) width per unit time (b) thickness per unit time (c) sputtering rate per unit time (d) depositing rate per unit time	1

2. Attempt all parts:-

2.a.	Give two reasons silicon is the most common semiconducting material. (CO1,K3)	2
2.b.	Sketch a cubic unit cell and identify the <100> plane. (CO2,K1)	2
2.c.	List four differences between optical lithography and electron beam lithography? (CO3,K3)	2
2.d.	What is Ion-Implantation Technique? Discuss in brief. (CO4,K1)	2
2.e.	List the four functions of a semiconductor package. (CO5,K1)	2

SECTION-B 20

3. Attempt all parts:-

3.a. Answer any one of the following:-

3.a.(i)	Explain different Point defects. (CO1,K2)	4
3.a.(ii)	Differentiate between Dry and Wet Oxidation. (CO1,K3)	4

3.b. Answer any one of the following:-

3.b.(i)	Draw a sketch of a horizontal tube furnace and identify all the sections. (CO2,K2)	4
3.b.(ii)	Explain the primary and secondary flats for n type and p type wafers for <100> and <111> orientation. (CO2,K2)	4

3.c. Answer any one of the following:-

3.c.(i)	Give some differences between Hard Baking and Soft Baking. (CO3,K3)	4
3.c.(ii)	Discuss positive photo resist with suitable diagram. (CO3,K2)	4

3.d. Answer any one of the following:-

3.d.(i)	Write a short note on Vapour phase Epitaxy. (CO4,K2)	4
3.d.(ii)	Explain in detail Plasma enhanced CVD systems. (CO4,K2)	4

3.e. Answer any one of the following:-

3.e.(i)	What are the advantages of a sputter process compared to an evaporator process? (CO5,K3)	4
3.e.(ii)	Discuss the various applications of metallization. (CO5,K5)	4

SECTION-C 35

4. Answer any one of the following:-

4-a.	Sketch the CZ process and explain its various parts. Also write its advantages and disadvantages. (CO1,K3)	7
4-b.	Differentiate between: (a) Polycrystalline and a single crystalline material. (b) Intrinsic and extrinsic semiconductors. (CO1,K3)	7

5. Answer any one of the following:-

5-a.	Explain the preparation of wafers from the crystal Ingot. (CO2,K2)	7
5-b.	Sketch a neat diagram and explain fabrication process of a NMOS device.	7

(CO2,K2)

6. Answer any one of the following:-

6-a.	What are the differences between dry and wet etching? Explain with diagram.(CO3,K3)	7
6-b.	Explain Pattern Transfer Defects in detail. (CO3,K2)	7

7. Answer any one of the following:-

7-a.	Derive expressions for Fick's Second Law of Diffusion. (CO4,K5)	7
7-b.	Discuss Molecular Beam Epitaxy in detail with diagram. (CO4,K2)	7

8. Answer any one of the following:-

8-a.	Explain the various types of Pin -Through – Hole Package with the help of a neat diagram. (CO5,K2)	7
8-b.	Explain the various steps of CMOS transistor fabrication using n well technique with diagram. (CO5,K2)	7