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Printed Page:-3 **Subject Code:- AMTVL0102**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA
(An Autonomous Institute Affiliated to AKTU, Lucknow)
M.Tech
SEM: I - THEORY EXAMINATION (2025 - 2026)
Subject: Advanced Digital Design Using Verilog

Time: 3 Hours **Max. Marks: 70**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. *This Question paper comprises of* ***three Sections -A, B, & C.*** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*

2. *Maximum marks for each question are indicated on right -hand side of each question.*

3. *Illustrate your answers with neat sketches wherever necessary.*

4. *Assume suitable data if necessary.*

5. *Preferably, write the answers in sequential order.*

6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION-A 15

1. Attempt all parts:-

1-a. The full form of HDL is _____ (CO1,K1) 1

(a) Higher Descriptive Language
(b) Higher Definition Language
(c) Hardware Description Language
(d) High Descriptive Language

1-b. Posedge means _____ (CO2,K2) 1

(a) Transition from x to 1
(b) Transition from 0 to 1, x or z
(c) Transition from z to 1, x
(d) Transition from 1 to 0

1-c. Which of the following can have more than one driver? (CO3,K1) 1

(a) IN
(b) OUT
(c) INOUT
(d) BUFFER

1-d. State transition happens _____ in every clock cycle. (CO4,K2) 1

(a) Once
(b) Twice
(c) Thrice
(d) Four times

1-e. Which of the following is main advantage of Pipelining? (CO5,K1) 1

(a) Exception handling
(b) Sequential execution
(c) Parallel Processing
(d) None of the mentioned

2. Attempt all parts:-

2.a.	What is the difference between a=#10 b and #10 a=b? (CO1,K2)	2
2.b.	What is always statement? (CO2,K2)	2
2.c.	Define logic synthesis and simulation. (CO3,K2)	2
2.d.	Write down the conditions required for the synthesis of combinational circuit. (CO4,K2)	2
2.e.	Describe the concept of Pipelining. (CO5,K2)	2

SECTION-B 20

3. Attempt all parts:-

3.a. Answer any one of the following:-

3.a.(i)	Explain top-down design methodology with block diagram and example. (CO1,K2)	4
3.a.(ii)	What do you mean by Module Instantiation? (CO1, K2)	4

3.b. Answer any one of the following:-

3.b.(i)	Write verilog code for 1 bit comparator using dataflow modeling. (CO2,K3)	4
3.b.(ii)	Explain structured procedure statements in Verilog. (CO2,K2)	4

3.c. Answer any one of the following:-

3.c.(i)	Discuss continuous assignments, combinational always blocks, and case statements with examples. (CO3, K2)	4
3.c.(ii)	Develop a Verilog module that implements a NAND gate. (CO3,K3)	4

3.d. Answer any one of the following:-

3.d.(i)	Implement a 4:32 register bank in Verilog HDL. (CO4, K4)	4
3.d.(ii)	Describe MOS switch primitives and their role in transistor-level simulation.(CO4,K2)	4

3.e. Answer any one of the following:-

3.e.(i)	Write down the limitations of Pipelining. (CO5,K2)	4
3.e.(ii)	Develop a mathematical model for an n-stage instruction pipeline. (CO5,K4)	4

SECTION-C 35

4. Answer any one of the following:-

4-a.	Explain the declaration of constants, variables and signals in Verilog with example. (CO1,K2)	7
4-b.	Explain data types in Verilog with special reference to net types, reg type, and wire type.(CO1,K2)	7

5. Answer any one of the following:-

5-a.	Write Verilog code to find the first bit with a value 1in Flag = 16'b 0010_0000_0000_0000. (CO2,K3)	7
5-b.	Write Verilog dataflow description of 1 Bit full adder. (CO2,K3)	7

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6. Answer any one of the following:-

6-a.	Write Verilog code to implement a **D flip-flop with synchronous reset**. (CO3,K3)	7
6-b.	Write a verilog code for priority encoder and explain with a neat block diagram. (CO3,K3)	7

7. Answer any one of the following:-

7-a.	Write and explain Verilog code for a finite state machine (FSM). (CO4,K3)	7
7-b.	Explain the data-path and controller design methodology. (CO4,K2)	7

8. Answer any one of the following:-

8-a.	Explain the implementation of a classic 5-stage RISC pipeline. (CO5,K2)	7
8-b.	Design a Verilog code for clocking issue in Pipeline. (CO5,K3)	7