.

Printed Page:-3 **Subject Code:- AMTVL0101**

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA
(An Autonomous Institute Affiliated to AKTU, Lucknow)
M.Tech
SEM: I - THEORY EXAMINATION (2025 - 2026)
Subject: CMOS Digital VLSI Design

Time: 3 Hours **Max. Marks: 70**

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*
1. *This Question paper comprises of* ***three Sections -A, B, & C.*** *It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.*
2. *Maximum marks for each question are indicated on right -hand side of each question.*
3. *Illustrate your answers with neat sketches wherever necessary.*
4. *Assume suitable data if necessary.*
5. *Preferably, write the answers in sequential order.*
6. *No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.*

SECTION-A 15

1. Attempt all parts:-

1-a. The enhancement type basically termed as normally-OFF N MOSFET works only with _____. (CO1,K2) 1

(a) large positive gate voltage
(b) large negative gate voltage
(c) large positive drain voltage
(d) large negative drain voltage

1-b. CMOS has (CO2, K2) 1

(a) high noise margin
(b) high packing density
(c) high power dissipation
(d) high complexity

1-c. PTL with single NMOS transistor has (CO3, K1) 1

(a) large node capacitance
(b) small node capacitance
(c) large node resistances
(d) small node resistances

1-d. In NORA CMOS logic___ is/are there. (CO4, K2) 1

(a) Charge sharing problem
(b) Charge sharing and leakage problem
(c) only leakage problem
(d) None of these

.

1-e.	Which of the following memories uses one transistor and one capacitor as basic memory unit (CO5,K2) (a) SRAM (b) DRAM (c) Both (d) None	1

2. Attempt all parts:-

2.a.	Explain the three regions of operation of a MOSFET. (CO1,K2)	2
2.b.	Explain Threshold voltage in CMOS inverter. (CO2, K2)	2
2.c.	Explain the working of CMOS NOT gate. (CO3, K2)	2
2.d.	Differentiate between synchronous and asynchronous sequential circuits. (CO4, K3)	2
2.e.	Give some applications where Flash memories are being used. (CO5, K4)	2

SECTION-B 20

3. Attempt all parts:-

3.a. Answer any one of the following:-

3.a.(i)	Explain the energy band diagram for combined MOS system and elaborate why there is bending near the oxide semiconductor interface? (CO1,K2)	4
3.a.(ii)	Explain Y-chart in detail. Define all the three domains involved in it. (CO1, K2)	4

3.b. Answer any one of the following:-

3.b.(i)	Explain briefly the scaling in VLSI. (CO2, K2)	4
3.b.(ii)	Why CMOS inverter power dissipation is low? (CO2, K3)	4

3.c. Answer any one of the following:-

3.c.(i)	Explain why NMOS is used in pull down network and PMOS is used in pull up network with the help of an example.(CO3,K2)	4
3.c.(ii)	What do you understand by OAI logic? Explain with the help of an example. (CO3,K2)	4

3.d. Answer any one of the following:-

3.d.(i)	Discuss the operation of pass transistor in dynamic logic circuit. (CO4,K3)	4
3.d.(ii)	Explain the concept of CMOS transmission gate logic in dynamic circuits. (CO4,K3)	4

3.e. Answer any one of the following:-

3.e.(i)	What is DRAM ? Explain DRAM with the diagram.(CO5,K2)	4
3.e.(ii)	Discuss and write operation of basic SRAM cell in detail. (CO5,K2)	4

SECTION-C 35

4. Answer any one of the following:-

4-a.	Explain CMOS n-well fabrication process with diagram. (CO1,K2)	7
4-b.	Explain gradual channel approximation and also derive expression for drain current in linear, saturation and cutoff regions. (CO1,K5)	7

5. Answer any one of the following:-

5-a.	What is CMOS inverter? Draw the voltage transfer curve (VTC) and explain.	7

.

(CO2,K3)

5-b.	Implement the following expression in a full static CMOS logic fashion : (CO2,K4) Y' = (A.B)+(D.E)+(D.C.B)	7

6. Answer any <u>one</u> of the following:-

6-a.	Explain the design of CMOS Full Adder with the help of a neat diagram. (CO3,K4)	7
6-b.	Discuss the CMOS implementation of SR latch and Verify its truth table. (CO3,K4)	7

7. Answer any <u>one</u> of the following:-

7-a.	What are the synchronous dynamic circuit techniques?Explain the performance of Domino CMOS logic with suitable example. (CO4,K3)	7
7-b.	Construct a logic function Z = { (E +F +G) (H+ I)}' using Pseudo nMOS logic, draw its diagram. (CO4,K4)	7

8. Answer any <u>one</u> of the following:-

8-a.	Distinguish between NOR flash memory cell and NAND flash memory cell. (CO5,K2)	7
8-b.	Explain about various sources of leakage current in memories.(CO5,K2)	7