Printed Page:-04 Subject Code:- BCSBS0303

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech

SEM: III - THEORY EXAMINATION (2024- 2025)

Subject: Computer Organization & Architecture

Time: 3 Hours Max. Marks: 100

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. This Question paper comprises of three Sections -A, B, & C. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.

2. Maximum marks for each question are indicated on right -hand side of each question.

3. Illustrate your answers with neat sketches wherever necessary.

4. Assume suitable data if necessary.

5. Preferably, write the answers in sequential order.

6. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION-A 20

1. Attempt all parts:-

1-a. Brain of computer is _____(CO1,K2) 1

(a) Control unit

(b) Arithmetic and Logic unit

(c) Central Processing Unit

(d) Memory

1-b. The smallest unit of data in computer is _____.(CO1,K2) 1

(a) Byte

(b) Nibble

(c) Bit

(d) KB

1-c. If A and B are the inputs of a half adder, the sum is given by _____(CO2,K2) 1

(a) A AND B

(b) A OR B

(c) A XOR B

(d) A EX-NOR B

1-d. Convert (52)base of 16 into its decimal equivalent.(CO2,K2) 1

(a) 28

(b) 83

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(c) 82

(d) N.O.T

1-e. For vertical microprogrammed control unit, n control signal requires……..bit encoding.(CO3,K2) 1

(a) log2n

(b) n-1

(c) 2^n

(d) log2n-1

1-f. Which of the following is the fastest type of memory in the memory hierarchy.(CO3,K2) 1

(a) Cache Memory

(b) Main Memory

(c) Secondary Storage

(d) Register

1-g. The _____ input is used by the DMA controller to request the CPU to relinquish control of the buses.(CO4,K2) 1

(a) Bus Grant

(b) Bus request

(c) Burst Transfer

(d) Data Input

1-h. UART stands for _____.(CO4,K2) 1

(a) Universal Asynchronous Receiver Transmitter

(b) Universal Asynchronous Relay Transmission

(c) Universal Accumulator Register Transfer

(d) None

1-i. Each stage in pipelining should be completed within _____ cycle.(CO5,K2) 1

(a) 1

(b) 2

(c) 3

(d) 4

1-j. _____ have been developed specifically for pipelined systems.(CO5,K2) 1

(a) Utility software

(b) Speed up utilities

(c) Optimizing compilers

(d) None of the mentioned

2. Attempt all parts:-

2.a. Explain the function of Stack pointer (SP) and program counter (PC).(CO1,K2) 2

2.b.	Explain universal logic gates with truth table.(CO2,K2)	2
2.c.	Give classification of memory.(CO3,K2)	2
2.d.	Define Input-Output Interface and its advantage.(CO4,K2)	2
2.e.	Explain types of Pipeline.(CO5,K2)	2

SECTION-B 30

3. Answer any five of the following:-

3-a.	Define bus arbitration and Explain the various types of bus arbitration techniques.(CO1,K3)	6
3-b.	Define Instruction format and Instruction cycle.(CO1,K2)	6
3-c.	Write the short notes on ALU and design 2 bit ALU Design in digital computer.(CO2,K3)	6
3-d.	Draw array multiplier of 2 bit, A=a1a0, B=b1 b0 .(CO2,K3)	6
3.e.	How the mapping is done between cache and main memory. Explain associative and Set-associative mapping.(CO3,K3)	6
3.f.	Define DMA. Explain DMA transfer in a computer system with the help of diagram.(CO4,K3)	6
3.g.	Write short notes on Single-instruction, single-data (SISD) systems.(CO5,K2)	6

SECTION-C 50

4. Answer any one of the following:-

4-a.	Draw the Multiple Bus structures along with its advantage and disadvantage.(CO1,K2)	10
4-b.	Define three state buffers and Draw the common bus architecture by using three state buffer.(CO1,K2)	10

5. Answer any one of the following:-

5-a.	Design the 4 bit Integer addition and subtraction with suitable diagram.(CO2,K3)	10
5-b.	Explain the IEEE 754 floating point representation for floating point numbers with examples.(CO2,K3)	10

6. Answer any one of the following:-

6-a.	Write a program to evaluate the arithmetic expression by using Three, and Zero address instruction. X=(A+B) * (C+D). (CO3,K3)	10
6-b.	Explain one address & two address instruction with example.(CO3,K2)	10

7. Answer any one of the following:-

7-a.	Explain the difference between program controlled, interrupt driven and DMA mode of data transfer.(CO4,K3)	10
7-b.	Explain the following with respect to DMA transfer: a) Bus request and Bus grant b)Burst Transfer c) Cycle stealing(CO4,K3)	10

8. Answer any one of the following:-

8-a.	Design and explain the concept of Pipelining with the help of suitable	10

example.(CO5,K2)

8-b. Define five pipeline stages in computer architecture and explain with the help of block diagram.(CO5,K2) 10

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