NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA
(An Autonomous Institute Affiliated to AKTU, Lucknow)
B.Tech
SEM: III - THEORY EXAMINATION (2024- 2025)
Subject: Logic Design and Computer Architecture

Time: 3 Hours   Max. Marks: 100

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*
1. This Question paper comprises of three Sections -A, B, & C. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.
2. Maximum marks for each question are indicated on right -hand side of each question.
3. Illustrate your answers with neat sketches wherever necessary.
4. Assume suitable data if necessary.
5. Preferably, write the answers in sequential order.
6. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION-A   20

1. Attempt all parts:-

1-a.   The output of two input OR gate is high ony if _____. (CO1,K2)   1

   (a)   both inputs are high

   (b)   both inputs are low

   (c)   atleast one of the input is high

   (d)   None of these

1-b.   Flip flop is a type of _____ circuit. (CO1,K2)   1

   (a)   Adder

   (b)   Sequential

   (c)   Combinational

   (d)   None

1-c.   What connects the various functional units of a digital system? (CO2,K3)   1

   (a)   Registers

   (b)   Flip-Flop

   (c)   Buses

   (d)   Multiplexer

1-d.   The third state of a Three-state Buffer is _____. (CO2,K3)   1

   (a)   0

   (b)   High Impedance

   (c)   1

    (d)   Short circuit

1-e.   How many address bits are required to represent a 32 K memory? (CO3,K4)   1

    (a)   10 bits

    (b)   12 bits

    (c)   14 bits

    (d)   15 bits

1-f.   The ALU gives the output of the operations and the output is stored in the _____. (CO3,K4)   1

    (a)   Memory Devices

    (b)   Registers

    (c)   Flags

    (d)   Output Unit

1-g.   Which type of memory is at the top of the memory hierarchy? (CO4,K5)   1

    (a)   Main memory

    (b)   Cache memory

    (c)   Registers

    (d)   Secondary storage

1-h.   What is the locality of reference? (CO4,K5)   1

    (a)   The phenomenon where data is randomly accessed.

    (b)   The tendency of a program to access a relatively small portion of memory repeatedly.

    (c)   The property of accessing all memory locations equally.

    (d)   The process of saving data to the hard disk.

1-i.   Which of the following is an example of a peripheral device? (CO5,K5)   1

    (a)   CPU

    (b)   External Memory

    (c)   RAM

    (d)   ALU

1-j.   Which of the following defines synchronous communication? (CO5,K5)   1

    (a)   Data is sent without a clock signal

    (b)   Data is sent with the help of a clock signal

    (c)   Data is transferred one bit at a time

    (d)   Data is transferred in parallel

2. Attempt all parts:-

2.a.   What do you mean by register and enlist its types? (CO1,K2)   2

2.b.   What are the functions of ALU and Control Unit? (CO2,K3)   2

2.c.   What are the roles of ALU ? (CO3,K4)   2

2.d.   Define the term 'hit ratio' and its significance in the context of memory   2

hierarchy.(CO4,K5)

2.e. Why parallel processing is important? (CO5,K5) 2

SECTION-B 30

3. Answer any <u>five</u> of the following:-

3-a.	Explain AND, NOR and XOR logic gates with the help of diagram and truth table.(CO1,K2)	6
3-b.	Explain the various types of sequential circuits. (CO1,K2)	6
3-c.	Draw the basic functional units of a computer and explain each of them. (CO2,K3)	6
3-d.	Explain the architecture of a system bus with a detailed description of the data, address, and control buses. (CO2,K3)	6
3-e.	Differentiate between RISC and CISC instructions with help of example. (CO3,K4)	6
3.f.	How does an SSD work and what are the components involved in its operation? (CO4,K5)	6
3.g.	How can pipeline hazards be resolved or minimized? (CO5,K5)	6

SECTION-C 50

4. Answer any <u>one</u> of the following:-

4-a.	What is Latch? Explain SR Latch in detail. (CO1,K2)	10
4-b.	Explain the working of 4:1 MUX and 1:4 DEMUX. (CO1,K2)	10

5. Answer any <u>one</u> of the following:-

5-a.	Explain the push and pop operations of register stack and memory stack with the help of a diagram. (CO2,K3)	10
5-b.	Explain the different types of addressing modes with its suitable example. (CO2,K3)	10

6. Answer any <u>one</u> of the following:-

6-a.	Discuss the key points of division algorithm and perform the division operation of 01110 by 10001 using division algorithm. (CO3,K4)	10
6-b.	Explain the working of 4 bit Carry Look Ahead Adder with help of example. (CO3,K4)	10

7. Answer any <u>one</u> of the following:-

7-a.	Explain the chip interconnections when 1024 X 8 memory is constructed using 128 X 8 RAM chips and 512 X 8 ROM chips. (CO4,K5)	10
7-b.	Explain the need of page replacement algorithm. Consider the page reference string 5,0,1,2,0,3,2,0,3,4,1,0,5,0,4,3,2,1,2,0,1 with 3-page frames. Find number of page faults using LRU page replacement algorithm. (CO4,K5)	10

8. Answer any <u>one</u> of the following:-

8-a.	Describe the different types of pipeline hazards. How do these hazards impact the performance of pipelined processors? (CO5,K5)	10
8-b.	Explain the need of strobe control and Handshaking and also draw its timing	10

diagram. (CO5,K5)

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