Printed Page:-03 Subject Code:- AEC0502

Roll. No:

NOIDA INSTITUTE OF ENGINEERING AND TECHNOLOGY, GREATER NOIDA

(An Autonomous Institute Affiliated to AKTU, Lucknow)

B.Tech

SEM: V - THEORY EXAMINATION (2024 - 2025)

Subject: CMOS Digital Integrated Circuit

Time: 3 Hours Max. Marks: 100

General Instructions:

IMP: *Verify that you have received the question paper with the correct course, code, branch etc.*

1. This Question paper comprises of three Sections -A, B, & C. It consists of Multiple Choice Questions (MCQ's) & Subjective type questions.

2. Maximum marks for each question are indicated on right -hand side of each question.

3. Illustrate your answers with neat sketches wherever necessary.

4. Assume suitable data if necessary.

5. Preferably, write the answers in sequential order.

6. No sheet should be left blank. Any written material after a blank sheet will not be evaluated/checked.

SECTION-A 20

1. Attempt all parts:-

1-a. What does MOSFET stands for? (CO1,K1) 1

(a) Metal Oxide Semiconductor Field Effect Transistor

(b) Modern Oxidized Silicon based Field Effect Transistor

(c) Modern Oxidized Silicon based Force Effect Transistor

(d) Metal Oxide silicon Field Equivalent Transistor

1-b. In which region, MOSFET perform as a switch? (CO1,K1) 1

(a) Cut-off

(b) Linear

(c) Saturation

(d) Option 1& 2

1-c. Pull-down network (PDN) connects output node to _____ . (CO2, K1) 1

(a) VDD

(b) Ground

(c) Input

(d) All of these

1-d. Which of the following CMOS logic circuits will contain parallel NMOS transistors? (CO2,K1) 1

(a) NOR

(b) NAND

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(c) NOT

(d) Transmission gate

1-e. The pass transistor logic often uses fewer transistors, run faster, and requires _____. (CO3,K1) 1

(a) More Power

(b) Less Power

(c) Zero Power

(d) Infinite Power

1-f. During precharge phase, PMOS transistor conduct and _____. (CO3,K1) 1

(a) Charge capacitance

(b) Discharge capacitance

(c) Charge inductance

(d) Discharge inductance

1-g. Hierarchical decomposition of a large system in VLSI design is called…….. (CO4,K1) 1

(a) Modularity

(b) Regularity

(c) Locality

(d) Decomposability

1-h. In which design all circuitry and all interconnections are designed? (CO4,K1) 1

(a) full custom design

(b) semi-custom design

(c) gate array design

(d) transistor design

1-i. An ASIC stands for _____ . (CO5,K1) 1

(a) American Specific Instruction code

(b) Application Specific Integrated Circuit

(c) Application Specific Instruction Code

(d) American Standard input Code

1-j. Input and output pads are made up of _____ . (CO5,K1) 1

(a) polysilicon

(b) metal

(c) silicon

(d) carbon

2. Attempt all parts:-

2.a. Explain accumulation mode in MOSFET. (CO1,K1) 2

2.b. Why multiplexer is called data selector circuit? (CO2,K1) 2

2.c. Define domino logic. (CO3,K2) 2

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2.d.	What is the standard cell-based ASIC design? (CO4,K1)	2
2.e.	What is do you mean by global routing? (CO5,K2)	2

SECTION-B 30

3. Answer any five of the following:-

3-a.	Design XOR gate using CMOS logic circuit. (CO1,K3)	6
3-b.	Derive the expression for dynamic power dissipation in CMOS inverter.(CO1,K2)	6
3-c.	Design D flip flop using CMOS. Discuss the importance of clock in a sequential circuit design.(CO2,K3)	6
3-d.	Explain Successive Approximation Register (SAR). (CO2,K2)	6
3.e.	Design a 4 to1 MUX using CMOS transmission gate. (CO3,K3)	6
3.f.	Draw the Layout Diagram of 2 input CMOS NAND gate. (CO4,K2)	6
3.g.	Explain in brief the floorplanning and placement in ASIC design. (CO5,K1)	6

SECTION-C 50

4. Answer any one of the following:-

4-a.	Why scaling is required in VLSI chips? And also explain different scaling methods of MOSFET. (CO1,K2)	10
4-b.	Explain the voltage transfer characteristics curve of CMOS inverter and explain different regions of operation. (CO1,K2)	10

5. Answer any one of the following:-

5-a.	Realize SR Flip Flop using CMOS and discuss its working. (CO2,K3)	10
5-b.	Explain the weighted resistor type and R-2R type DAC. (CO2,K2)	10

6. Answer any one of the following:-

6-a.	Design three input NOR gate using Pseudo-NMOS and explain its operation. Briefly mention its advantages and disadvantages with respect to the static CMOS.(CO3,K3)	10
6-b.	How to prevent the charge sharing problem in domino logic? Explain in detail. (CO3,K2)	10

7. Answer any one of the following:-

7-a.	Explain λ-based design rules in VLSI circuit design. (CO4,K2)	10
7-b.	Draw a stick diagram for CMOS logic Y= (A+B+C)'. (CO4,K3)	10

8. Answer any one of the following:-

8-a.	Draw and explain in detail the ASIC design flow. (CO5,K2)	10
8-b.	Explain in detail the two major checks before fabrication. (CO5,K1)	10