1. MICROWIND 3.8- Advance CMOS Layout design & Simulation Tool with FinFET 14 nm Technology

- Library based schematic editor with facility to create symbols.
- Library of various digital models like gates, registers, 74xx series devices, etc.
- Both conventional pattern-based logic simulation and intuitive on-screen mouse-driven simulation.
- Supports hierarchical logic design with built-in extractor which generates a SPICE netlist from the schematic diagram (compatible with pSpice and WinSpice)
- Generation of Verilog description of the schematic for layout generation.
- MOS level schematic support.
- Fault analysis tool at the gate level of digital circuits. Faults: Stuck-1, stuck-at-0.
- Immediate access to symbol properties of models like delay, fanout.
- Models and assembly support for 8051 and PIC 16F84 with facility to simulate with external circuits.
- Sub-micron, deep-submicron, nanoscale technology support.
- Facility to list delays of path and support critical path analysis.
- User-friendly advance CMOS layout design and simulation tool with FinFet technology support.
- FinFet device support with 2D cross section, 3D visualization, and layout construction.
- Design-error-free cell library (contacts, vias, MOS devices, etc.)
- Facility to convert CMOS layout in schematic, compatible with DSCH.
- Advanced macro generator: MOS, capa, matrix, ROM, pads, path, etc..)
- Ease in navigation for very large designs.
- Incredible translator from logic expression into compact design-error free layout
- Powerful automatic compiler from Verilog circuit into layout.
- Verilog compiler with various automatic routing methods like standard and compact.
- On-line design rule checker: width, spacing, overlap, extension rule verification
- Built-in extractor which generates a SPICE netlist from layout
- Extraction of all MOS width and length
- Parasitic capacitance, crosstalk and resistance extracted for all electrical nodes
- Import/Export CIF layout from 3rd party layout tools
- Lock & unlock layers to protect some part of the design from any changes
- Enhanced editing commands and layout control
- Built-in SPICE-like analog simulator features fast time-domain, voltage and current estimation, with very intuitive post processing: frequency estimation, delay estimation. (No external SPICE/ analog simulator.)
- Supports LEVEL1, LEVEL3 and BSIM4 models for all technologies from 1.2µm down to 14nm FinFET.
- MOS characteristic viewer, with access to main model parameter
- Real-case measurement data-base in 0.7,0.35, 0.25 and 0.18µm for comparison with models
- The ability to label nodes allows intuitive control of the simulation (supply, clock, pulse, PWL, sinus, maths)

- Time-domain voltage and current waveforms available at the press of one single icon
- DC/AC characteristics, signal frequency vs. time, eye diagrams
- Min/Typ/Max analog simulation
- Convenient Monte-carlo simulation
- Powerful fast-Fourier Transform to support radio-frequency circuit simulation
- On screen Power estimation
- Storage of simulation results in external CSV file format.
- Sophisticated parametric simulation to investigate the effect of several key parameters on the circuit performances: R,L,C, temperature, supply voltage, etc.
- Huge device simulation model library
- Inbuilt interconnect analyzer to compute field between ground planes and conductor
- MOS characteristics viewer with the model parameters and visualization of their effects on Id/Vd, Id/Vg Id(log)/Vg, threshold vs Length
- 3D fabrication process simulator with cross sectional viewer, facility to select different layers for visualization.
- Visualization of contacts and metallization created
- Checking of the self-aligned diffusion after the polysilicon gate is fabricated
- Check planes of VDD, VSS, and others signals
- Check the oxide structure, the low dielectric (Low K) and high K (SiO2) sandwich, and passivation
- User can check the gate oxide and the MOS lateral drain diffusion structure
- Simulation of non-volatile memories such as EPROM, EEPROM and FLASH using double-gate MOS
- Erasure of floating gates and removal all electrons.
- Full length tutorial on MOS models is provided in manual, with details on all parameters
- Supports 1,3 and BSIM4 MOS models
- 200-pages documentation including several aspects of logic design
- More than 200 basic circuits ready to simulate
- To be supplied with WinSpice Simulator, for third party simulation of examples.

2. Multi-Vendor PLD platform for VLSI Front end design

Multi vendors FPGA - Basic foundation board should consist of different peripherals & interfacing accessories.

- Spartan 6 FPGA - XC6SLX9-2TQG144C: The XILINX Spartan-6 FPGA device with: Operating Frequency: 50MHz; Operating Voltage: 1.15V～3.3V; Package: QFP144, I/Os: 102; Logic Cells: 9152, RAM: 132kb; Debugging/Programming: supports JTAG with USB JTAG must be provided.
- Altera Cyclone IV EP4CE6E22C8N - P4CE6E22C8N: the ALTERA Cyclone IV FPGA device which features: Operating Frequency: 50MHz; Operating Voltage: 1.15V～3.465V; Package: QFP144; I/Os: 80; LEs: 6K; RAM: 270kb; PLLs: 2; Debugging/Programming: Supports JTAG with USB JTAG must be provided.

Basic foundation board must consists of;

- 8 Bit ADC 0804
- 8 Bit DAC using 0808
- 16 Digital Inputs through switches & 16 LED's for Output for any logical experimentation
- 16x2 LCD display
- 4 Digit 7 segment display
- 4x4 Keypad
- DC Motor control drivers with motors
- Stepper Motor control drivers with motors
- Relay Buzzer & LED sequence
- 2 serial ports
- VGA Port.

Interfaces must be provided such as;

- 128x64 Graphics LCD (GLCD)x1,
- AT45DBXX DataFlash Board x 1,
- FM24CLXX FRAM Board x 1,
- PCF8563 RTC x1,
- PCF8591 AD DA Board x 1,
- Temperature sensor DS18B20 x 1,
- USB to UART converter with USB Micro interface,
- ENC28J60 Ethernet Board x 1,
- FPGA's must be provided and should be interchangeable with foundation board.
- All required Cables, connectors, Power adaptor.

3. Xilinx - Vivado Design Suite HLx Editions

The Vivado® Design Suite offers a new approach for ultra-high productivity with next generation C/C++ and IP-based design with the new HLx editions including HL System Edition, HL Design Edition and HL WebPACK™ Edition.

For High Level Design

- Software-defined IP Generation with Vivado High-Level Synthesis
- Block-based IP Integration with Vivado IP Integrator
- Model-based DSP Design Integration with System Generator for DSP

For Verification

- Vivado Logic Simulation
- Integrated Mixed Language Simulator
- Integrated & Standalone Programming and Debug Environments
- Accelerate Verification by >100X with C, C++ or SystemC with Vivado HLS

For Implementation

- 4X Faster Implementation
- 20% Better Design Density
- Up to 3-Speedgrade Performance Advantage for the low-end & mid-range and 35% Power Advantage in the high-end